Topics in Analysis and Design of Primary Parallel Isolated Boost Converter

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Ph.D. Thesis

Topics in Analysis and Design of Primary Parallel Isolated Boost Converter

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Preface

This PhD project, “Flexible power module for fuel cell hybrid power system in a fork-lift,” is carried out under the PhD research program EnergyLabDK at the PhD school, Department of Electrical Engineering, at Technical University of Denmark (DTU), and cooperated with H2Logic A/S in Herning, Denmark. This project has also been supported by Advanced Technology Foundation (HTF) in Denmark. During this project, a research visit is carried out at Istanbul Technical University and Marmara Research Center, Istanbul, Turkey.

During the course of this PhD study, I have received help and support from a number of people. I would like to mention their names in here to show my appreciation to them.

- My supervisors Michael A. E. Andersen and Ole C. Thomsen have continuously supported me throughout this project with their kind attitude, constructive feedback and encouragement.
- H2Logic A/S supported this project and my colleagues over there, Lars Møller and Rasmus Refshauge, were actively involved in the process with both their technical abilities and positive attitude.
- I have been a part of DTU Electronics Group during my PhD study and it has always been a source of happiness and inspiration for me. With its friendly environment, intelligent members and up-to-date facilities, I strongly believe that our group will continue to produce high quality research and make much more contribution to the power electronics literature.
- Throughout my PhD project, I have collaborated with Kristian Lindberg-Poulsen, Juan C. Hernandez B., Maria C. Mira A., Ziwei Ouyang and M. Seyed Dehghan D., with whom I have co-authored the papers presented in this thesis. I extremely enjoyed to do research with these smart people and learned a lot from them.
- My parents Osman and Serap, my lovely wife Busra and my little son Mehmet Akif have been a source of my motivation. They stood by me during both good and hard times.

Thanks everyone!

Abstract

Efficient power processing through power electronics circuits has been a popular academic field for the past decades, especially after “green” vehicle applications based on fuel cells, batteries and super-capacitors emerged as alternative sources of propulsion for transportation. Dc-to-dc converters found their places in such applications as voltage / power regulators where relatively lower voltages with higher currents are to be handled. Among various converter topologies proposed and used in the literature, *Primary Parallel Isolated Boost Converter* (PPIBC) is a good candidate for such applications due to its simplicity and ability to handle higher currents.

Design of magnetic structures like transformers and inductors is part of power electronics engineering in which trade-offs exist between size, price and losses. In higher currents this becomes even more challenging since conventional wire wound design approach has some shortcomings. It is possible to use copper foil in windings however this will increase the amount of handcraft during manufacturing; so academic attention was needed for this part of low voltage high current switching converter design.

Planar magnetics and integration of magnetic components are becoming more widely used by switch mode designers since there is a trend towards high power density, high switching frequency and higher efficiency. Planar magnetic components are also suitable for Printed Circuit Board (PCB) compatible design which results in easier manufacturing. Integration of magnetic components together with planar magnetic technology offers unique solutions where some of the contributions of this thesis came from.

During this research the aim was to design a dc-to-dc converter module based on PPIBC topology for a fuel cell operated forklift manufactured by H2Logic A/S. This thesis is written based on the academic outcomes during this design process. Various aspects of PPIBC have been investigated and a number of contributions to the literature have been made.

- An integrated transformer structure has been proposed for PPIBC where modular design with less core volume and core loss due to flux cancellation has been obtained.
- An inductor with integrated current balancing transformer has been applied to PPIBC eliminating the need for a separate current balancing transformer.

- Transformers and inductors of a PPIBC have been integrated into a single magnetic structure.
- Different current balancing configurations for PPIBC have been investigated.
- A modeling approach to PPIBC has been proposed for closed loop control.
- A bidirectional version of PPIBC has been built and tested successfully.

Danske Resumè

Effektiv omformning af strøm ved hjælp af elektronikkredsløb har været et populært fagområde i de sidste årtier, især i kraft af "grønne" køretøjer baseret på brændselsceller, batterier og super-kondensatorer i forbindelse med brug af vedvarende energi til transport. DC-DC konvertere har fundet deres pladser i sådanne applikationer som konvertere, hvor relativt lave spændinger med højere strømme skal håndteres. Blandt forskellige konverter topologier der er foreslået og anvendt i litteraturen, er Primary Parallel Isoleret Boost Converter (PPIBC) er en god kandidat til sådanne applikationer på grund af sin enkelhed og evne til at håndtere større strømme.

Design af magnetiske strukturer i transformatorer og spoler er en del af effektelektronik, hvor afvejninger skal gøres mellem størrelse, pris og energitab. Ved højere strømme dette bliver endnu mere udfordrende, da konventionelt trådviklet design har en del mangler. Det er muligt at anvende kobberfolie i viklinger, men det vil øge mængden af manuelt arbejde under fremstillingen, derfor var en forskningsmæssig indsats nødvendig. Plane magnetiske strukturer og integration af magnetiske komponenter bliver mere og mere udbredt indenfor effektelektronikdesign, da der er en tendens i retning af høj effekttæthed, høj switchfrekvens og højere effektivitet. Plane magnetiske komponenter er også egnede til at lave på printkort, hvilket resulterer i lettere og billigere fremstilling. Integration af magnetiske komponenter sammen med plane magnetiske strukturer tilbyder unikke løsninger, hvortil denne afhandling bidrager. I løbet af denne forskning var målet at designe en DC-DC konverter modul baseret på PPIBC topologien til en brændselscelledrevet gaffeltruck fremstillet af H2Logic A/S. Denne afhandling er skrevet baseret på de faglige resultater i løbet af dette forskningsprojekt. Forskellige aspekter af PPIBC er blevet undersøgt, og en række forskningsmæssige bidrag er fremkommet:

- En integreret transformer struktur er blevet foreslået for PPIBC, hvor modulært design med mindre kernevolumen og kernetab som følge af udbalancering af fluxen er opnået.
- En induktor med integreret strømbalanceringstransformer til PPIBC eliminerer behovet for en separat strømbalanceringstransformer.
- Transformatorer og spoler til PPIBC er blevet integreret i et enkelt magnetisk struktur.

- Forskellige aktuelle balanceringskonfigurationer til PPIBC er blevet undersøgt.
- En modelleringstilgang til PPIBC er blevet foreslået for lukketsløjferegulering.
- En tovejs version af PPIBC er blevet bygget og testet med succes.

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Chapter I : Introduction

1.1 Scope

The scope of this report is to present the results obtained in the PhD project "Flexible power module for fuel cell hybrid power system in a fork-lift," performed by the author during the period from December 2008 through June 2012 in collaboration with H2Logic A/S. Many of the scientific results obtained in the project is published in the form of conference and journal papers and a patent application. The published papers form an integral part of this thesis and are included in appendix [A1]-[A11]. The objective of this report is to supplement the already published information by placing the published papers in the context of the overall project and thereby present a more coherent and complete overview of the work and results obtained.

1.2 Background and Motivation

Power electronics is still continuing to be a popular field among electrical engineers due to the increased demand for renewable alternatives for energy production and consumption. Efficient and compact power electronic converters are being requested from designers which drives the need for new converter topologies as well as new technologies of manufacturing including component level. If an application requires higher currents to be handled, some challenges appear regarding efficiency, thermal design and component size. In case of magnetic component design and manufacturing, as the current level increases, standard wire wound designs become insufficient in terms of current carrying capability. This forces designers to use copper foil together with interleaved arrangement of windings to overcome skin and proximity effects reducing the conduction losses.

Recently significant contribution has been made to the literature both in efficient dc-dc converter design [29] and PCB based planar integrated magnetics [62]. Primary parallel isolated boost converter (PPIBC) which is proposed in [29] is a simple and very efficient candidate for low voltage and high current applications with a reported maximum efficiency of 98.2%.

1.3 Project Objectives

Magnetic component design in switch mode power converters is a critical stage which may considerably affect the overall performance and competence of the end product. One of the objectives of this research project is to investigate potentials of using planar magnetics for magnetic components of PPIBC, which is a modular and low profile technology. In addition possibilities of merging magnetic components are inspected.

Necessity of a current balancing mechanism adds an extra magnetic component to PPIBC. This component is a current balancing transformer (CBT) in the original design. In this thesis alternatives to CBT are investigated including integrated magnetic solutions.

Accurate modeling of dc-dc converters is necessary in order to be able to design a stable controller. It is also important to include target load type in the model since it may change the converter dynamics significantly. In this thesis a small signal model is derived based on non-ideal components, in order to investigate the dynamic behavior of PPIBC as a battery charger.

Bidirectional dc-dc converters together with batteries and super-capacitors are commonly used in electric/hybrid propulsion systems as peak energy shavers and regenerative energy capturers. PPIBC can be an efficient alternative for this purpose with its high current handling capability since peak shaving applications require high current handling in short time. One of the objectives of this research is to design and implement a bidirectional PPIBC loaded with batteries. Boost type dc-dc converters have startup problem and limited input/output voltage range. Overcoming this limitation is possible by modifying the input inductor and employing additional circuitry. Alternative configurations for extended voltage operation and startup for PPIBC is explored as part of this project.

1.4 Thesis Structure

Fig.1 shows the structure of this thesis. Chapter II gives a brief state-of-the-art discussion, showing the frame where the thesis contribution is made. Chapters III and IV summarizes the contribution of the research with reference to the publications [A1] – [A11] given in appendix.

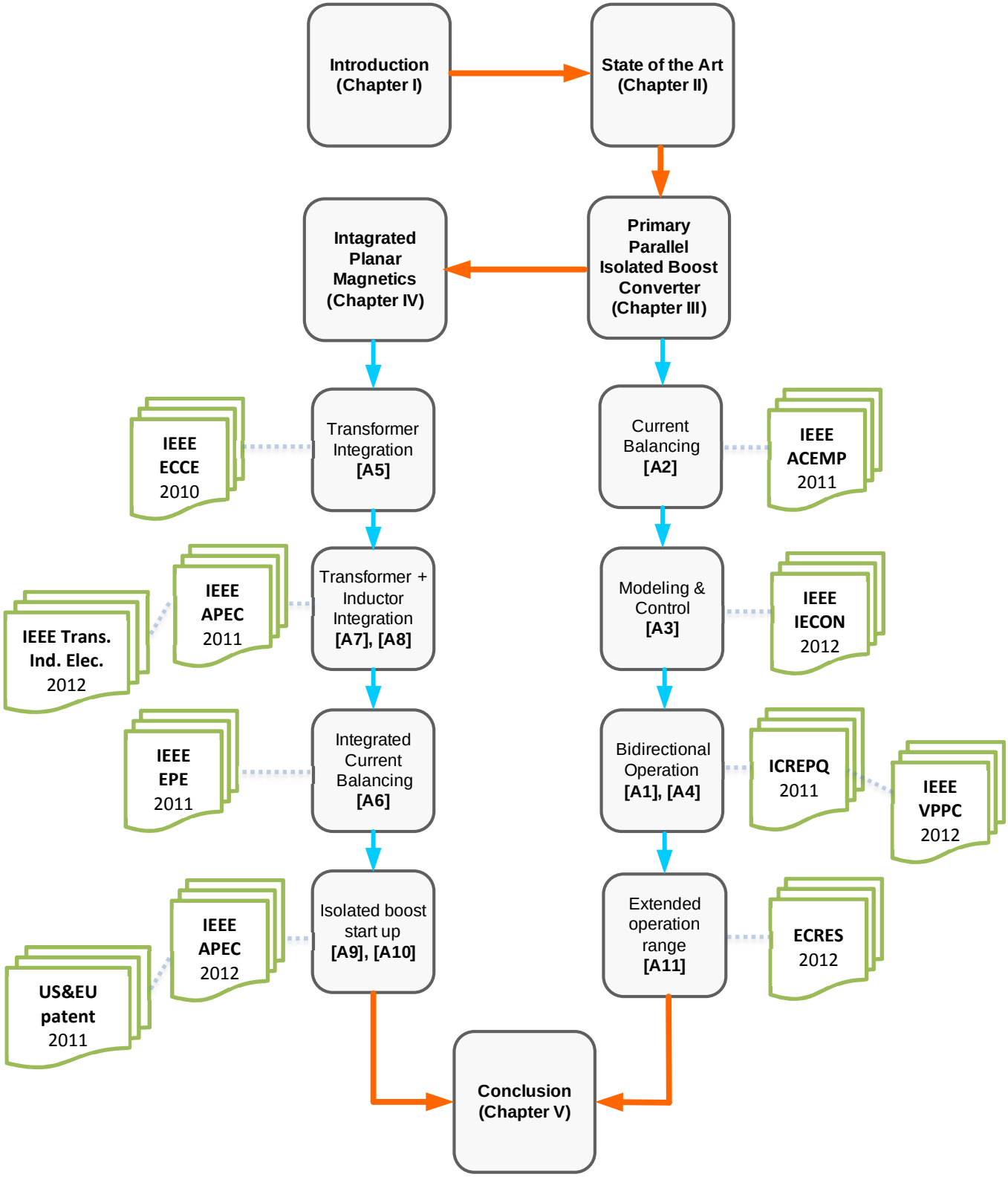


Figure 1 PhD thesis structure related to the publications

Chapter II : State-of-the-Art

2.1 Introduction

Significant research has been accomplished related to dc-dc converters for fuel cell and battery applications by researchers. New topologies are emerging some of which draw attention and address some common requirements of dc-dc converters such as higher efficiency, compact design and lower price. Even if they have satisfactory performance in laboratory conditions, where they are tested with power supplies at the input and resistor banks at the output, their input and load configuration for the end application should also be taken into consideration. Therefore characteristics of fuel cells and batteries as well as system architectures including one or more of these energy storage elements are of interest for power electronic designers.

In this chapter, first a brief introduction to fuel cells and batteries is given by referring to related publications. Then different system configurations for interfacing the fuel cell to the rest of the system are mentioned. Since giving detailed analysis of these energy storage devices are out of scope of this thesis, reader is encouraged to go through the literature for detailed information.

Next, dc-dc converters for fuel cell applications in the literature have been introduced with reference to the analysis made in [29]. Important factors affecting efficiency have been mentioned and listed based on the previous research. Lastly, based on the summarized arguments regarding high efficiency, critical points on magnetic component design are given especially related to ac resistance and leakage inductance.

2.2 Fuel Cell Power System

Fuel cell is a device for electro-chemical energy transformation, first demonstrated in 1839 by William Grove [1]. It became more popular in the last decade among energy related engineering areas due to the need for alternative energy resources. Fuel cells are good candidates for this purpose because they work based on the clean process of inverse electrolysis. However hydrogen should also be produced based on renewable energy for a completely “green” cycle. Eq. (1) shows the basic equation for this process.

$$H_2 + \frac{1}{2}O_2 = H_2O + Electical\ Energy + Heat \quad (1)$$

One way of classifying fuel cells is based on the type of electrolyte used. The following is a list of the fuel cell types and operating temperatures [2]:

- Alkaline fuel cells (AFCs) , 50-200 ^{o}C
- Phosphoric acid fuel cells (PAFCs), 220 ^{o}C
- Proton exchange membrane fuel cells (PEMFCs), 30-100 ^{o}C
- Molten carbonate fuel cells (MCFCs), 650 ^{o}C
- Solid oxide fuel cells (SOFCs), 500-1000 ^{o}C

A basic diagram of a fuel cell loaded through a power electronics converter is shown in Fig.2. Hydrogen, produced by the reformer, is applied to the anode and it is separated into electrons and hydrogen ions. While positive hydrogen ions travel through the membrane (polymer electrode); electrons follow the electrical route to the cathode. After recombining with the oxygen and hydrogen ions, water is formed [2].

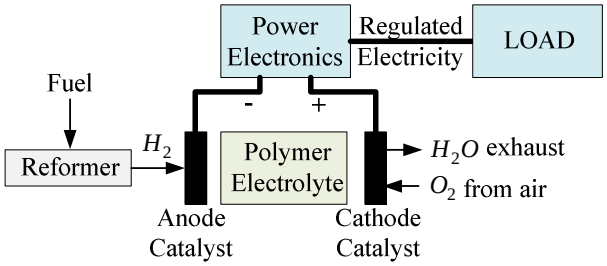


Figure 2 Basic diagram of a loaded fuel cell system

Fuel cell is different from a battery except both have terminals with a dc operating voltage. As long as the Hydrogen is supplied, electrical power is produced in a fuel cell stack, avoiding any long charge time as in the case of a battery. Electrical behavior of a fuel cell stack is also quite different from that of a battery in terms voltage – current dependency of the device. The “piecewise” behavior of the fuel cell voltage depending on current is given in Fig.3. Different regions are dominated by different types of loss, namely activation loss, Ohmic loss and concentration (transport) loss [3].

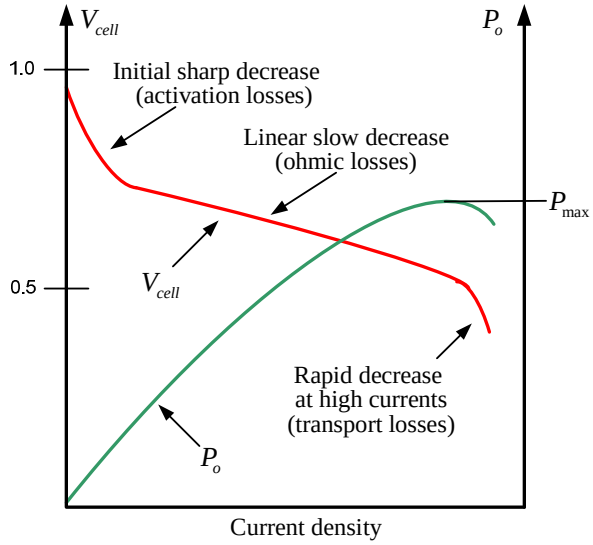


Figure 3 Typical fuel cell V-I curve with output power

Among different types of fuel cells, PEMFC has been rapidly developed as the primary power source in FC vehicle propulsion and distributed generation applications, because of its high energy density, low working temperature, and simpler structure [4]. Most fuel cells designed for usage in vehicular applications are less than 1.16 volts. This is far from producing enough voltage for a vehicle. Therefore, multiple fuel cells must be series connected to form a fuel cell stack. The power generated by a fuel cell stack depends on the number and size of each cell that comprises the stack and its surface area [5].

Power electronics, which interfaces the fuel cell stacks and the rest of the power system, should be designed considering some important electrical features of the fuel cell system such as V-I relationship and aging effect. Both the current drawn from the cell and the age of the cell has an effect on the terminal voltage. This results in ~50% variation in input voltage to the power electronics converter affecting the component sizing and losses. Also the low frequency ripple on the fuel cell current is not recommended since it reduces the fuel cell efficiency and lifetime [6], [7]. However high frequency switching ripple can easily be filtered by the local filter capacitors at the input of the converter as well as the capacitive nature of the fuel cell due to the phenomena of “charge double layer” [8]. Ripple currents with frequencies above 400 Hz have minor impact on the fuel cell stack’s operation and a ripple factor of less than 4% has negligible impact on the conditions within the fuel cell diffusion layer. Thus it does not significantly affect the fuel cell’s lifetime [17].

Similar to the low frequency ripple limitation, a slew rate limitation also applies to the terminal current of the fuel cell stack [9]. This is due to the difference between the time constants of the mechanical and electrical phenomena in a fuel cell system. Since the mechanical time constants are in the order of seconds, they dominate the dynamic behavior and the response time. Lastly, most fuel cell stacks today are unidirectional. In case of a current direction change or a sudden stop in the current drawn, the fuel cell terminal voltage increases. In this case the Hydrogen supplied should be decreased immediately and a dummy load should be activated in order not to overstress the components. In some applications a diode is connected in series with the fuel cell stack terminals to avoid reverse current flow at the expense of increased conduction losses.

In many applications fuel cell based power systems also include secondary energy storage units such as batteries and super-capacitors. This is due to the need for supporting the fuel cell system during start up and transients; since fuel cell has slower dynamics. Especially during start up significant delay occurs due to the power up of the mandatory components of operation, the pumps, heat exchangers, and fuel processing unit which are called the balance-of-plant (BOP).

2.3 Batteries for Electric Vehicles

Batteries dedicated to electric vehicle propulsion are of rechargeable type with higher ampere-hour and deep cycle capability compared to starting-lighting-ignition (SLI) type batteries [10]. They are used for a wide range of vehicular applications including forklifts, golf carts, electric motorcycles, full-size electric cars and trucks. EV batteries are expected to have some features in order to be competitive in this area:

- Higher power and energy density
- Longer cycle life time
- Higher charging current rating
- Wider operating temperature
- Smaller self-discharge
- Lower cost

Different types/technologies for EV batteries are available with their pros and cons [11]. Among them lead-acid batteries seem to be a simple, mature technology and a cost effective choice. They are still being improved for higher power and longer lifetime. Lead-acid batteries are available from a wide range of suppliers and considered to be safe since they have been used as starting-lighting-ignition purposes for a long time in automotive applications. However their high weight being (25–50%) a portion of the final vehicle mass and short cycle life time remains to be a disadvantage.

Another commonly preferred battery type in EV applications is nickel metal hydride (NiMH). It has a relatively less charging-discharging efficiency (60-70%) compared to lead-acid batteries. However they have an energy density value up to 120Wh/kg which is much better than lead-acid types (up to 40Wh/kg). NiMH type batteries have long life times and have been used in commercial hybrid cars like RAV4EV. The drawbacks of NiMH are their poor efficiency and high self-discharge.

ZEBRA (Na-NiCl2) batteries are of molten salt type, operating at higher temperatures up to 700 ^{o} C. They have a high energy density of 120Wh/kg with a reasonable internal resistance due to the insolubility of the electrodes. The main disadvantages appears to be the high operating temperate (270°C) and poor power density (<300W/kg).

Lithium-ion (Li-ion) batteries also draw attention especially in recent EV developments. They are one of the most popular types of rechargeable batteries with one of the best energy density figures (up to 250Wh/kg), efficient charge-discharge cycles, and a small self-discharge when not used. New generation Li-ion batteries are being developed for EV applications which sacrifice energy and power density in order to obtain fire safety, fast charging and longer life time. There are commercial examples of Li-ion usage for EVs including Tesla Roadstar EV having a range of more than 200 miles [12].

Fig.4 shows different battery technologies as well as the super-capacitor technology compared with respect to their specific power and specific energies. Lithium based technologies seem to be very promising. Lead-acid type batteries have poor performance leaving their price and wide availability as advantage. Super-capacitors may find their shares in an EV application as peak shavers regarding their high current/power capability.

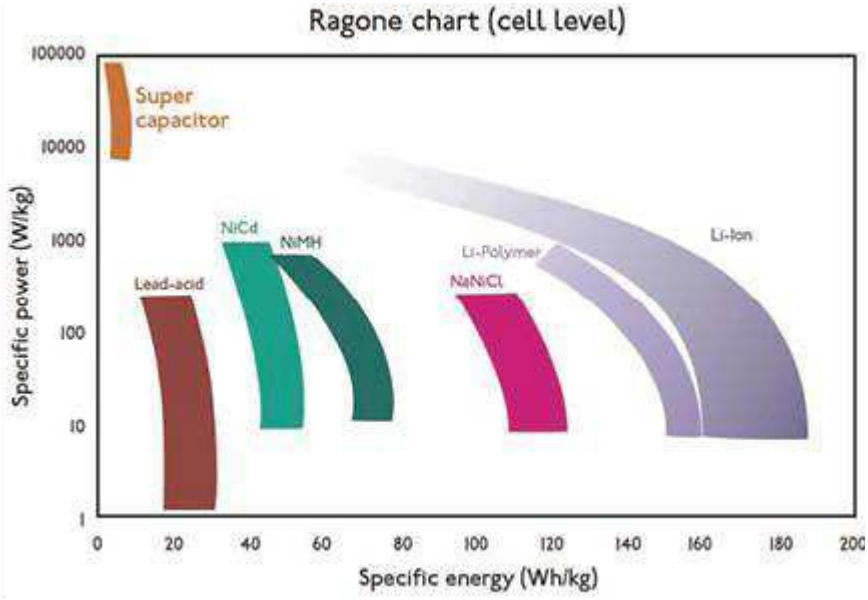


Figure 4 Power vs. energy density of different battery types [11]

2.4 Fuel Cell Interfacing Methods

Using auxiliary energy storage units like battery and/or super-capacitor in combination with fuel cells is necessary and commonly preferred in vehicle applications as well as grid connected applications [13]-[17]. Slow and current dependent nature of the fuel cell voltage requires leveling and power demand filtering. Recovering the braking energy in vehicle applications is also a reason for secondary energy storage with bi-directional power electronics interfacing.

Various interfacing methods have been used by designers so far some of which are shown in Fig.5. The configurations in Fig.5 (a) and (b) are based on a common dc bus voltage where both energy sources are regulated. The two energy sources are practically decoupled which gives the freedom of separated power management and size optimization. Regarding the fast dynamics of the converters, constant and stable dc bus can be assured as long as the dc-dc converters are well regulated. Increased number of units and lowered efficiency are the drawbacks for the configurations in Fig.5 (a) and (b).

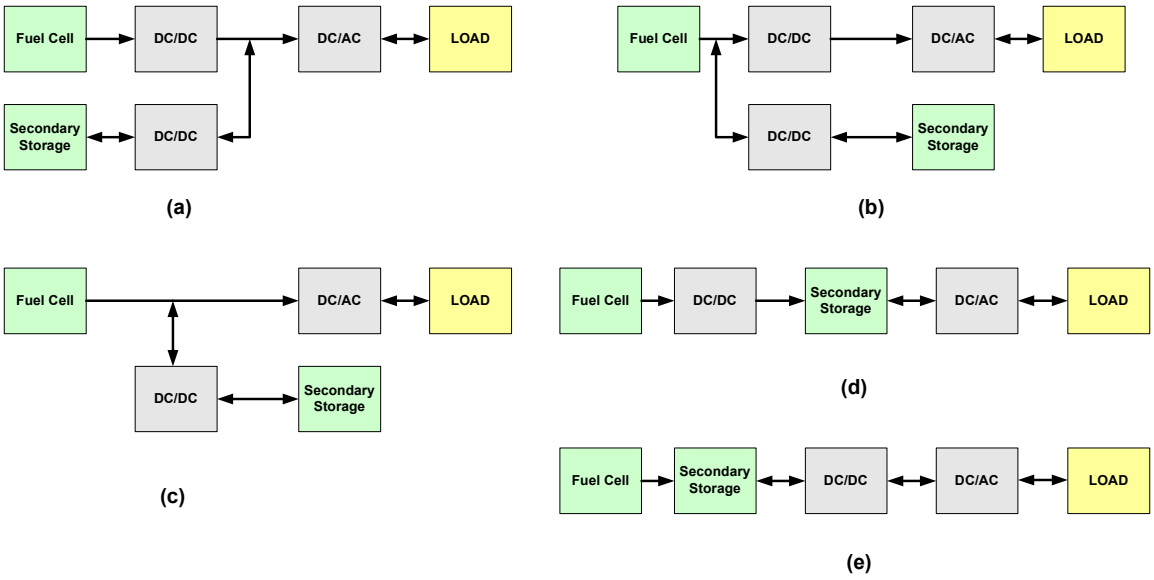


Figure 5 Possible interfacing methods of a fuel cell stack and a secondary energy storage device

The configuration shown in Fig.5 (c) is based on a fuel cell dependent bus voltage where the secondary storage is connected through a bi-directional dc-dc converter. Fluctuations in the power demand from the load side are managed by the secondary energy storage unit; so a proper controller with enough bandwidth is required for the dc-dc converter. Possible variations in the dc bus voltage can also be a challenge for the load side dc-ac converter design. The advantage of this case seems to be the possibility of optimum sizing of the secondary energy storage unit and eliminating the fuel cell dc-dc converter which has a non-ideal efficiency.

Fig.5 (d) is a commonly preferred simpler and cheaper architecture compared to Fig.5 (a). The dc bus is fixed to the secondary storage voltage and the fuel cell is coupled to the system through a dc-dc converter. The advantage of controlling the fuel cell terminal voltage/current is preserved. However direct connection of the secondary storage to the dc bus before the dc-ac converter may prevent optimum usage of the secondary storage element and oversize the selection of its parameters.

In Fig.5 (e), the secondary storage element which in this case is generally a super-capacitor bank, is directly connected to the fuel cell terminals. It mostly behaves as a decoupling capacitor bank, shaving the power demand peaks. This configuration prevents full utilization the super-capacitor whose steady state voltage is determined by the fuel cell voltage. Another

problem here is the possible uncontrolled current variations of the fuel cell depending on the impedance of the connection in between.

Some dc-dc converter topologies are suitable for multi-input connection [18]-[24]. This allows combining two sources in one power electronics structure. Depending on the design of multi-input dc-dc converter, it may end up being a compact system since there are common units such as control, output or filtering stages. Some of these converters are obtained by series connection of the input stages of dc-dc converters [23], while others use galvanic isolation in the form of multi-winding transformers in order to couple different input sources [24].

2.5 Fuel Cell DC-DC Converter

As explained in the previous chapter, fuel cell has a unique electrical output characteristic which requires interface electronics with a certain control strategy for proper operation. So far, many dc-dc converter topologies have been proposed in the literature which can be categorized in different classes like isolated/non-isolated, buck/boost type.

In case of the non-isolated converters, boost derived topologies dominate the literature since fuel cell applications generally require stepping up the voltage. If high step up is needed, simple boost converter may not be the best choice since duty cycle may approach to extreme values [25]. In order to obtain higher voltage gain, coupled inductors and capacitive voltage doublers have been used [26]-[28]. The drawbacks of these approaches are the possible increases in switch voltage stress and switching losses due to the leakage inductance of the coupled inductor.

Isolated dc-dc converters solve the voltage gain problem. They have both buck type and boost type alternatives for fuel cell applications. The high frequency transformer used for galvanic isolation is also used as voltage level shifter avoiding extreme duty cycles and impractical topologies to achieve high gain. Isolated dc-dc converters in the range of 1kW-10kW suitable for fuel cell applications are investigated and compared in [29]. Following isolated dc-dc topologies are reported and commonly preferred:

- Isolated push pull converter [30]-[32]
- Isolated two inductor boost converter [33]-[39]

- Isolated buck converter [40]-[44]
- Isolated boost converter [45]-[51]

In these papers, different efficiency values for various power levels are presented. In [29], it is reported that following points are in general believed to be the main obstacles for achieving high efficiency in isolated dc-dc converter design among some power electronics designers:

- High current and/or high turns-ratio transformers tend to have high leakage inductances which cause the significant part of the switching losses.
- In isolated boost type converters, due to the high voltage spikes, primary switch voltage ratings should be much higher than the nominal voltage reflected over them.
- Voltage clamp circuits should be employed.
- In order to increase the efficiency, soft switching topologies should be preferred especially in low voltage applications.

In [52], it is demonstrated that it is possible to achieve efficiencies up to 98% in a low input high output voltage application without taking into consideration the above statements. Furthermore some of those statements were shown to be wrong like the turns ratio and leakage inductance relationship, while some others are not necessarily true for all applications like the necessity for soft switching and high voltage rating requirement for primary switches. In order to achieve good efficiency figures other factors should be considered including topology selection [53]. In [29], these factors were summarized as follows:

- Substantial interleaving is required both for reducing the conduction losses in the transformer due to the proximity effect and obtaining low leakage inductance which reduces the switching losses.
- Power stage layout is very critical in high current switching applications. Low stray inductance and ac resistance should be targeted.
- Voltage clamp circuits become unnecessary in a low leakage/stray inductance design, since they also have their own parasitic inductances which prevent them filtering the voltage spikes appearing over the switches.

2.6 Considerations in Magnetic Components Design

Switch mode circuit designers have some degree of freedom in magnetic component design compared to other discrete components in the circuit since it is not possible to change a parameter inside a MOSFET or an electrolytic capacitor. In case of a transformer, it is possible to arrange the winding structure and change the transformer parameters such as dc and ac resistance, leakage inductance and inter-winding capacitance [54]. In [52], it has been shown that it is very critical to select the correct transformer winding arrangement in low voltage - high current dc-dc converters. Transformer conduction losses, which are directly proportional to the square of the pulsating winding current, tend increase significantly if a non-interleaving winding arrangement is preferred. Different winding arrangements with different leakage inductance and ac resistance values are investigated in [52] for a standard core structure and in [54] for a planar core.

AC resistance of a transformer winding layer is a factor of layer thickness (h), skin depth (δ) and the degree of interleaving (m) which is related to the contribution of the proximity effect. Based on the work of [55] and [56], Eq. (2) shows the normalized ac resistance with respect to the dc resistance of a winding layer [25].

$$F_R = \frac{R_{AC}}{R_{DC}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi - \cos 2\varphi} + \frac{2(m^2 - 1)}{3} \varphi \frac{\sinh \varphi - \sin \varphi}{\cosh \varphi + \cos \varphi} \tag{2}$$

The variable φ is defined as $\varphi = h/\delta$.

$$m = \frac{F(h)}{F(h) - F(0)} \tag{3}$$

Here $F(h)$ and $F(0)$ are the MMF values at the limits of a layer as shown in Fig.6. Eq. (2) can used to obtain the family of curves shown in Fig.7 where different ac resistance values are shown to exist for a layer depending on the above mentioned factors. It is obvious that significant changes in ac resistance may occur depending on the configuration. Each layer in Fig.6 has its own ac resistance value with respect to its location in the winding (m).

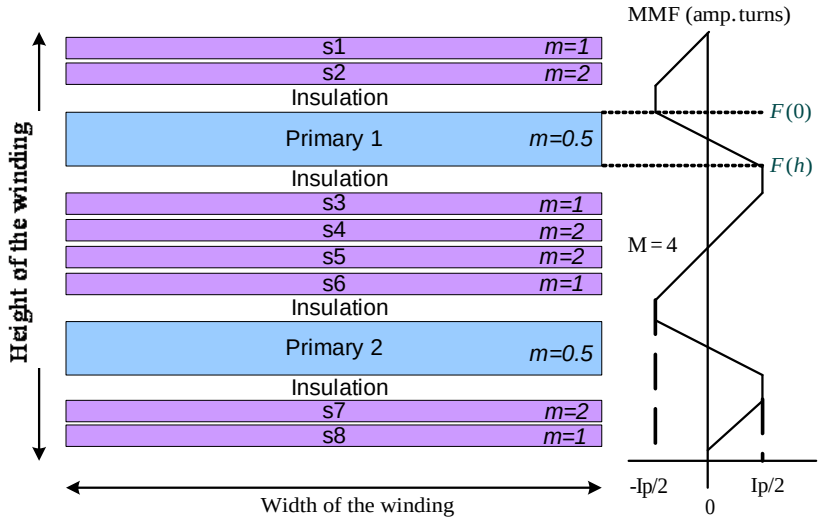


Figure 6 An example winding configuration with four primary-secondary intersections

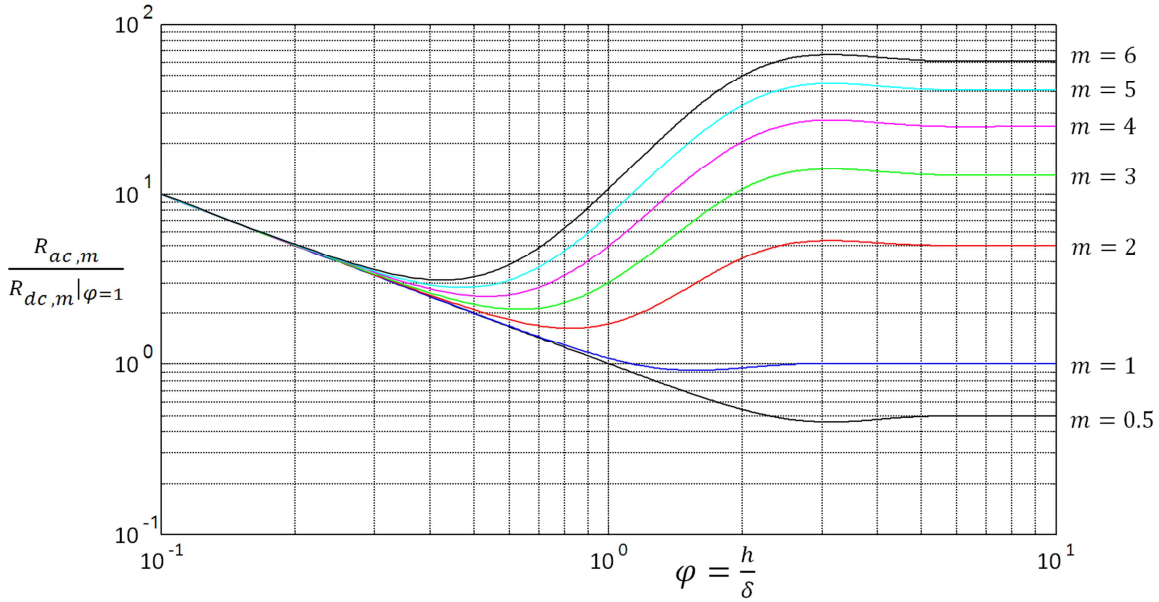


Figure 7 AC resistance of a layer normalized to its dc resistance when ϕ = 1 for different m values

Based on the work of [55] and [56], a simplified expression of leakage inductance value of a transformer has been derived in [29],

$$L_{LK} = \mu_o \frac{l_w h_w N^2}{3 b_w M^2} \tag{4}$$

In Eq. (4), l_w is the mean length of turn, h_w is the total height of the transformer winding, b_w is the breadth of the winding, N is the number of winding turns and M is the number of intersections between primary and secondary layers. Turns ratio of the transformer does not appear in the equation so the leakage inductance is independent of the turns ratio. On the

other hand, number of turns contributes with its square, which implies that in low voltage high current applications, since primary side has low number of turns, leakage energy which contributes to the switching losses tend to be lower due to the low leakage inductance value. However leakage energy is also related to the square of the current value at the switching instant which is the reason why winding configuration requires special attention.

In [52], four different cases have been compared in terms their leakage inductance and ac resistance values for a 1.5kW, 30-50V input, 400V output fuel cell dc-dc converter using simple isolated boost topology as shown in Fig.8. These windings have been wound on an EE55/21 ferrite E-core with a 45kHz frequency of current switching where the skin depth is 0.34 mm. Authors have used 0.6mm for primary side winding and 0.15mm for secondary side.

Table I summarizes the reported calculation results of the ac resistance and leakage inductance values for the above mentioned winding configurations in [52]. In Table I, $F_{R,P}$ is the ratio of ac resistance over the dc resistance or shortly ac resistance factor for the primary winding. Similarly, $F_{R,S}$ is the ac resistance factor for the secondary winding and $F_{R,T}$ is the transformer ac resistance factor. Also $L_{LK,P}$ and $L_{LK,S}$ are the primary and secondary winding leakage inductances. Based on these results, authors have selected case (d) for their application and built a transformer for experimental verification.

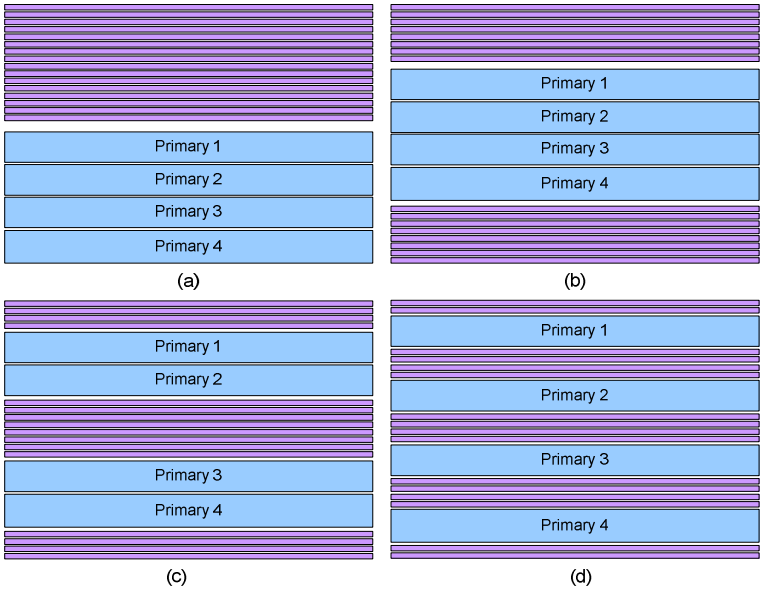


Figure 8 Four different winding configurations compared in [52], a) non-interleaving M=1, b) single interleaving M=2 c) double interleaving M=4, d) quadruple interleaving M=8

TABLE 1: CALCULATED PARAMETERS FOR FOUR DIFFERENT CONFIGURATIONS IN [52]

Winding configurations	(a)	(b)	(c)	(d)
M	1	2	4	8
$F_{R,P}$	13.3	3.96	1.63	1.05
$F_{R,S}$	2.07	1.27	1.07	1.02
$F_{R,T}$	7.7	2.6	1.35	1.04
$L_{LK,P}$ *(nH)*	249	70	21	7.2
$L_{LK,S}$ *(nH)*	3976	1114	339	115

In order to further interpret the ac resistance and leakage inductance results given in Table 1, they should be compared to the impedance level of the simple isolated boost converter designed in [52]. In [29], it has been pointed out that in low voltage and high current converter applications; impedance level of the converter which is given in Eq. (5) forms a basis for the other impedances in the circuit to be compared.

$$\mathrm{R_{in}} = \frac{V^2_{\mathrm{in}}}{P_{\mathrm{in}}} \tag{5}$$

Based on Eq. (5), input impedance of the converter in [52] for minimum input voltage (30V) can be obtained as $R_{in} = 0.6\Omega$. The measurements reported for the implemented transformer are 1.9mΩ ac resistance and 11nH leakage inductance (total series impedance 3.1mΩ @ 45 kHz) referred to the primary side. These values correspond to 0.32% and 0.52% of the converter input impedance (R_{in}), respectively. Based on an averaged converter steady state equivalent circuit, these percentages can be scaled with converter duty cycle which will correspond to the respective efficiency drops due to the conduction losses and inductive clamp losses assuming that all the leakage inductance energy dissipated. Similar to this procedure converter output impedance can be obtained ($R_{out} = 109\Omega$) to which secondary side series impedances can be normalized. As an example for case (d) in Table 1, $\frac{\omega_s L_{LK,P}}{R_{in}} = 0.34\%$ and $\frac{\omega_s L_{LK,S}}{R_{out}} = 0.03\%$ can be calculated which shows that primary impedances are 10 times more important that the secondary side impedances in terms effecting the losses. Table 2 gives the percentages of transformer ac resistance referred to primary side, $L_{LK,P}$ and $L_{LK,S}$ for different interleaving configurations in Fig.8. It is obvious from here that degree of interleaving has a significant impact on converter efficiency.

TABLE 2 RELATIVE TRANSFORMER IMPEDANCES FOR DIFFERENT CONFIGURATIONS IN [52]

Converter impedances	(a)	(b)	(c)	(d)
M	1	2	4	8
AC resistances based on M=8 measurement: 1.9mΩ (Normalized to R_{in} *)*	2.37%	0.8%	0.42%	0.32%
$L_{LK,P}$ *(Normalized to* R_{in} *)*	12%	3.37%	1%	0.34%
$L_{LK,S}$ *(Normalized to* R_{out} *)*	1.2%	0.33%	0.09%	0.03%

2.7 Summary of State-of-the-Art

This chapter briefly touches to the topics related to fuel cell dc-dc converters. Firstly, general information on fuel cell structure and types is given together with the electrical characteristics. Since fuel cell systems are generally used with secondary energy storage in vehicle applications, EV batteries are also introduced. Various fuel cell interfacing methods in the literature with their pros and cons are mentioned. Both isolated and non-isolated fuel cell dc-dc converter topologies are introduced and some of the topologies from literature are referenced. Finally, factors which are believed to affect the efficiency together with the factors which really affect the efficiency have been pointed out based on previous research.

Chapter III : Primary Parallel Isolated Boost Converter

3.1 Introduction

In this chapter first, the concept of "converter power scaling" will be introduced based on the discussions in [29]. Then primary parallel isolated boost converter (PPIBC) as a partial paralleling method for converter power scaling will be discussed with reference to the publications [59]-[61]. After that different current balancing methods mentioned in [61] will be analyzed and compared based on [A1] and [A2]. Later, based on the results presented in [A3], modeling and control of PPIBC will be briefly discussed. Finally PPIBC with bidirectional operation will be presented regarding the research results given [A1] and [A4].

3.2 Converter Power Scaling

Increasing the power level of a converter has practical limits like lower efficiency and increased thermal stress of the components. Fig.9 shows a typical efficiency curve of a dc-dc converter where at higher power levels there is a tendency to lower efficiency values due to the increased conduction (I^2R) losses. Further increase in power demand will practically require some sort of power scale up for the dc-dc converter [29].

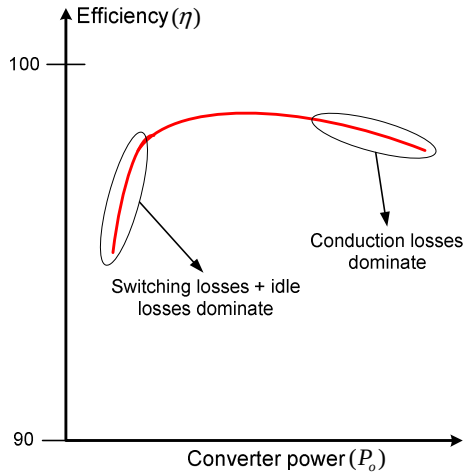


Figure 9 Typical efficiency curve of a dc-dc converter

A simple method for increasing power level is basically straight paralleling of dc-dc converters connecting their input and output terminals where additional control is required for power balancing. Since same modules will be paralleled, simple and cost-effective

manufacturing can be utilized; for example printed circuit board (PCB) based designs can be used. This will bring flexibility in power level as well as repeatability.

Interleaved or out-of-phase operation can also be employed for parallel connected dc-dc converter modules. This can reduce the input and output ripple values and significantly mitigate the filtering requirement since the effective ripple frequency will be multiplied by the number of parallel modules.

In [29], a different approach in dc-dc converter scaling has been given. Instead of module-wise parallel or series connection of converters, a “minimum paralleling approach” has been proposed. In this approach, scalability of each component of a dc-dc converter is questioned based on the simple isolated boost converter application. Following conclusions have been drawn:

- It is possible to design efficient high current inductors using double winding method up to 10kW [58]. This allows scaling up the inductor power level without any thermal stress and efficiency problems due to the high current and ac resistance.
- In order to keep the contribution of primary switch conduction losses the same, several switches should be connected in parallel. In case of low input voltage applications, MOSFETs are preferred as primary switches. Regarding the practical limits in dynamic current sharing due to the physical connections with different parasitic nature and the parameter tolerances of each component will make parallel connected operation difficult. Especially during inductive switching, sharing the leakage energy in the form of avalanche losses is not easy.
- Due to the ac nature of the transformer current and the frequency dependent limitation of copper penetration depth, increasing the amount of copper per winding does not help in conduction losses after a certain thickness except higher level of interleaving or paralleling the turns are employed. Both winding interleaving and paralleling has limitations of increased inter-winding capacitance and manufacturing complexity.
- Similar to the ac resistance and leakage inductance concerns in transformer design, inter-component connection should also be considered carefully from dc-dc converter scaling point of view. Especially high ac current loops in the circuit as shown in Fig.10 are prone to drastic increase in conduction losses as well as inductive switching losses since the stray inductance of the connections will be in series with

the leakage inductance of the transformer. An increase in power level, which will require an increase in physical size of the components, will lead to longer inter-component connections with higher ac resistance and leakage inductance.

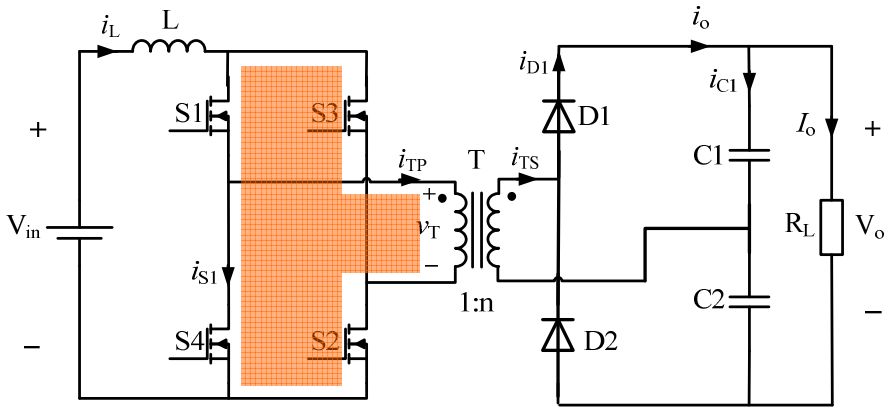


Figure 10 Simple isolated boost converter with voltage doubler and high ac current loop highlighted [52]

3.3 Scaling with Partial Paralleling

Based on the conclusions on component level scaling given in the previous section, the author of [29] proposed a new family of very high efficiency boost type isolated converter topologies built on simple isolated boost converter [59]-[61]. Fig.11 shows a two transformer variation of the topology which is named as “primary parallel boost converter” in the publications which will be referred as “primary parallel isolated boost converter (PPIBC)” in this thesis. The idea behind this topology is based on a minimum partial paralleling approach where only critical high current ac loops are paralleled and the rest of the circuit is scaled up according to the required power level. This keeps the topology simple while ensuring high efficiency and scalability [29].

The operation of the circuit in Fig.11 is similar to the one in Fig.10. Switches S1-S2 work synchronously with S5-S6 and switches S3-S4 work synchronously with S7-S8. Inductor L is charged when all the switches are in the on state and discharged when only diagonal pairs (S1-S2-S5-S6 or S3-S4-S7-S8) are in the on state. This way, transformers T1 and T2 also work synchronously and have the same flux pattern. The series connection of the transformer secondary windings forces the current to be equal during the inductor discharge phase which forms together with the current balancing transformer (CBT) T3, a balancing mechanism for the parallel full bridge-transformer combinations. T3 is practically an inverse coupled inductor acting as high impedance in case of a mismatch in switching times.

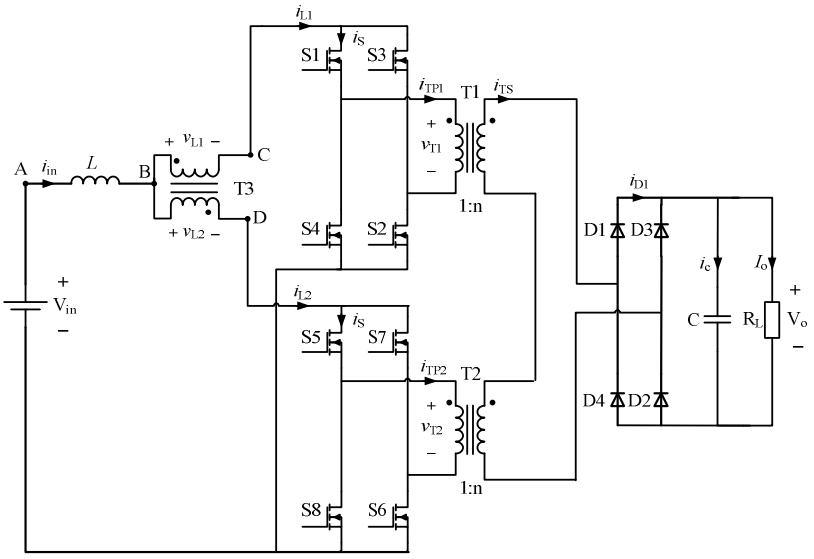


Figure 11 PPIBC with two transformers [59]

Steady state input and output voltage relationship can be derived as in Eq. (6),

$$\frac{V_o}{V_{in}} = \frac{n}{1-D} \tag{6}$$

where D is the switch duty cycle. As can be observed from Eq. (6), one other advantage of secondary series connection is the increase in the effective voltage conversion ratio compared to simple isolated boost converter with full bridge rectifier at the output without any increase in the turns ratio of individual transformers. This allows simpler transformers since lower number turns will be enough for the secondary side.

Dividing the high input current with a simple sharing mechanism at the low voltage primary side and increasing the voltage conversion ratio for the high voltage secondary side are the advantages of PPIBC. Variations of the topology are given in [61]. In [59], a two transformer, 3kW application is reported with an input voltage between 30-50V and an output voltage of 400V resulting in a peak efficiency of 98% at 50V input. In [60], a four transformer, 10kW PPIBC has been published with the same input voltage level, this time output voltage being 800V. A record efficiency of 98.2% has been reported.

3.4 Current Balancing Configurations

Based on the topology variations of PPIBC mentioned in [61], four different cases for current balancing has been investigated as part of this PhD study and published in [A1] and [A2]. In [A1], an early version of the current balancing analysis is given together with a bi-directional version of PPIBC. In [A2], a more detailed analysis is presented with analytical expressions derived for each case, supported with simulation and experimental results. Since the details can be found in appendix, only a summary of the analysis will be given in this section.

Fig.12 shows a switching instant for PPIBC in Fig.11 where one of the two full bridges is delayed in switching such that the upper full bridge connected to T1 is in energy transfer (or inductor discharging) mode while the lower one connected to T2 is trying to charge the input inductor. The current i_d represents the differential current flow from the upper full bridge to the lower due to the asymmetrical voltage reflection. This is an extra operation mode where voltage and current distribution in the circuit may change and cause unbalanced stress over the components. Considering the moment in Fig.12, after the switching transient effects, the output voltage which should normally appear across the secondary windings of the two transformers as $V_o/2$, now appears as complete V_o across the T1 secondary winding. Since in the lower full bridge, all the switches are in the on state, T2 secondary winding will practically be shorted. This may cause switches S1 and S2 having higher voltage stress during the mismatch time. Some current imbalance will also occur due to the fact that complete output voltage V_o, reflected through T1 will appear across T3 and cause the differential current id to flow from one branch to the other. The shorter the mismatch time and the higher the mutual inductance of T3, the lower will be the imbalance between the branch currents. If the mutual inductance of T3 is reduced to zero, then the only impedance limiting the rate of change of current id will be the stray inductance of the physical connections in the circuit.

Fig.13 (a) shows such a case where high di/dt can be observed during turn-on and turn-off times. If a CBT is employed, these current spikes are suppressed as seen in Fig.13 (b). The differences between the two scope images in Fig.13 can be analyzed together with the switching instant given in Fig.12. The current spikes of the two branches seen in Fig.13 (a) occur after a charging period where one branch current has a positive spike and the other one has a negative spike with the same magnitude. This implies the existence of the differential

current (i_d) which is driven by the reflected voltage (V_o/n) through the upper transformer. Depending on the magnitude of V_o, the value of the inductance (L_m) and the delay time, current spike magnitude will change. The value of L_m increases significantly if CBT is employed. This prevents the current spikes by keeping the magnitude of i_d significantly small since the rate of change of i_d depends on the impedance in series with the differential path.

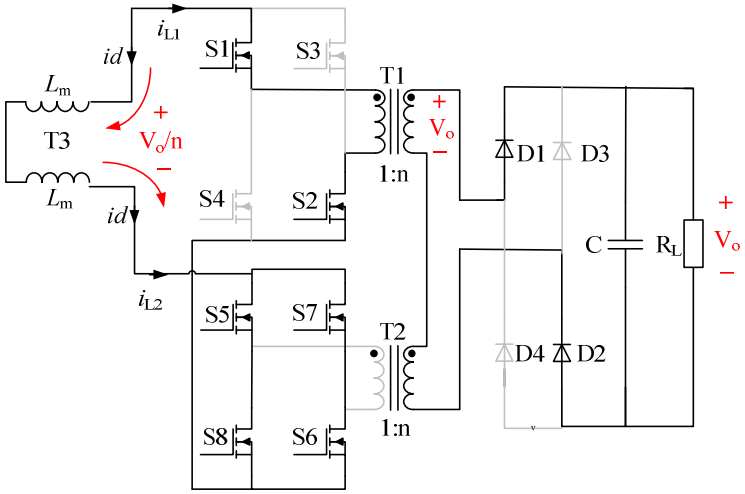
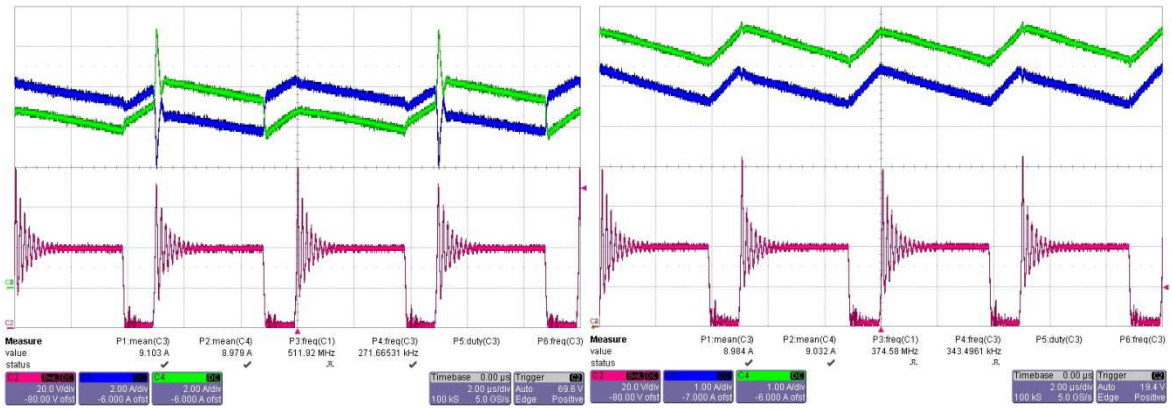


Figure 12 PPIBC with a switching time mismatch



(a) (b)

Figure 13 Measured branch currents (green and blue)

(a) with and (b) without CBT with common drain voltage (red) of the upper full bridge.

The analysis of branch currents for different current balancing configurations shown in [A2] is based on switching delay assumptions of two diagonal switches in one full bridge. Branch current difference expressions derived in [A2] are the results of either a turn-on or a turn-off delay. There may be different types of timing non-idealities such as mismatched duty ratios

or dead time / overlap time differences between the switches. There may even be different combinations of these timing non-idealities. However all these time mismatch combinations may only result in two extra operation modes, namely a “turn on delay” or a “turn off delay” as explained in [A2] where respective branch current difference expressions are given. The expressions for CBT case are repeated below in Eq. (7) and Eq. (8) for turn on and turn off delays, respectively. In these equations, d_{on} and d_{off} are the turn on and turn off delay times normalized to the switching period, respectively. K is the current difference between the two branches. It can be observed from the equations that the current imbalance is directly proportional to delay times and voltage value and inversely proportional to switching frequency and CBT impedance.

$$K = \frac{D\, d_{on} V_g}{2\, f_{SW} L_m (D' + d_{on})} \tag{7}$$

$$K = \frac{-d_{off}^2 V_g}{2D'\, f_{SW} L_m} \tag{8}$$

For instance a duty cycle mismatch case is shown in Fig.14 where lower full bridge switches have higher duty ratios than upper ones. As can be seen from the figure, two turn on delays for the upper full bridge and two turn off delays for the lower full bridge appeared per period. For this case a design criteria for the CBT can be obtained by considering Eq. (7) and Eq. (8) for a worst case duty ratio mismatch corresponding to a desired current imbalance limit.

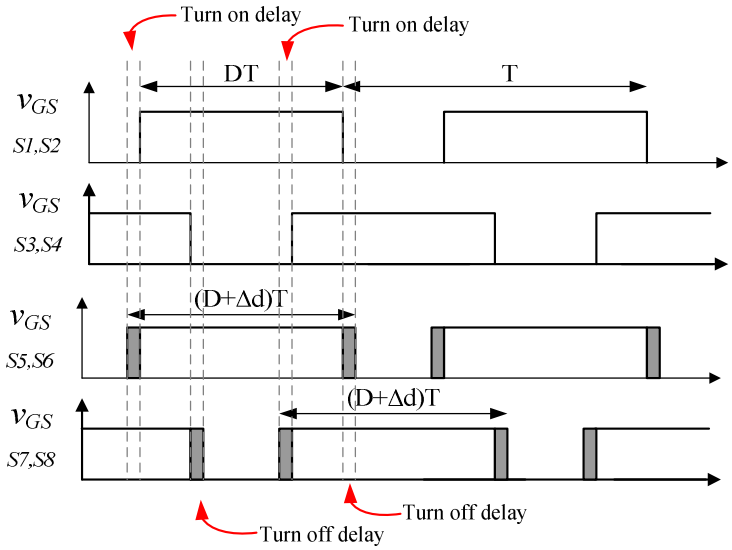
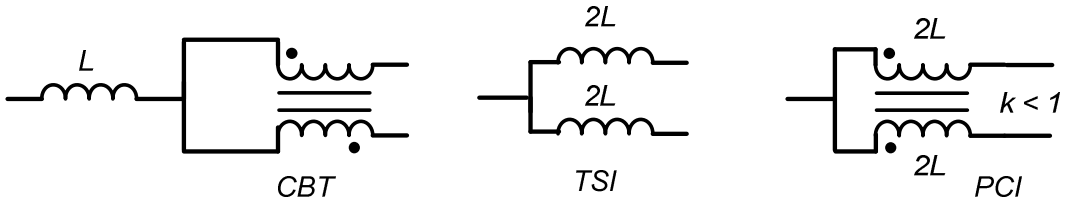


Figure 14 PPIBC gate signals with duty ratio mismatch between the two full bridges

It is also possible to have current balancing and energy storage combined. In [A2], two additional current balancing configurations, namely two separate inductors (TSI) and partially coupled inductor (PCI) are analyzed. Their circuit diagrams are shown in Fig.15 (b) and (c).

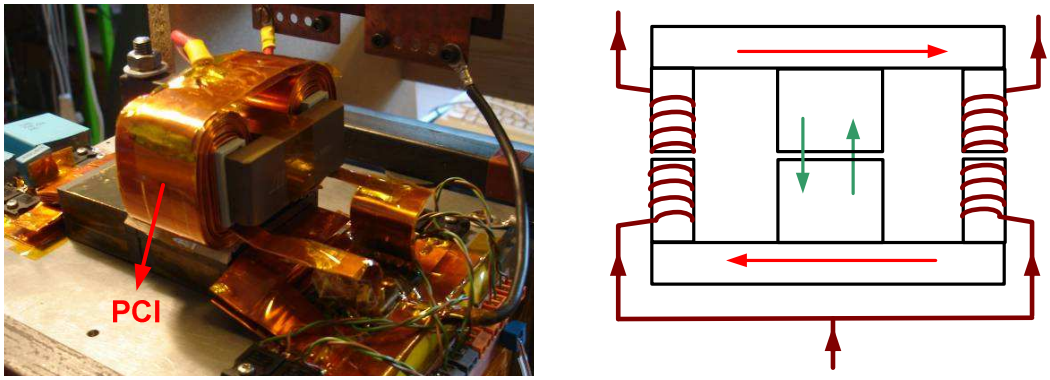


(a) (b) (c)

Figure 15 Circuit diagrams for three different current balancing configurations (a) current balancing transformer (CBT) in series with an inductor (b) two separate inductor (c) partially coupled inductor

In the case of TSI, instead of using a single inductor and a CBT, separate inductors are employed for each parallel full bridge-transformer combination. The advantage is that the input current is divided into two, relieving the current stress for the input inductors; however double the inductance is required for each inductor in order to keep the same input current ripple; since the two inductors are practically in parallel. Another drawback of TSI configuration is the inductance tolerance due to the core material and winding tolerances. Different inductances will cause different slopes in branch currents resulting in current imbalance. Winding tolerances may also cause different slopes for PCI configuration. However CBT is relatively less affected by these tolerances due to its practical implementation where high permeability cores can be used with minimum number of turns (including single turn).

It is also possible to merge energy storage and current balancing in the same component using PCI. It can be implemented using an E shape powder core with its side legs populated with a winding each as shown in Fig.16. PCI is composed of two loosely direct coupled inductors. In the center leg, which does not contain any windings, no flux flows as long as the branch currents in each winding are equal. In case of a current difference in the branches, causing a difference in flux, center leg will act as an alternative flux path which forms the necessary impedance for limiting the rate of rise of the differential current i_d.



(a) (b)

Figure 16 PPIBC with PCI used for current balancing (a) built with E core halves (b) basic diagram

In summary following points can be highlighted based on the discussion on current balancing configurations in this section as well as publications [A1] and [A2] in the appendix:

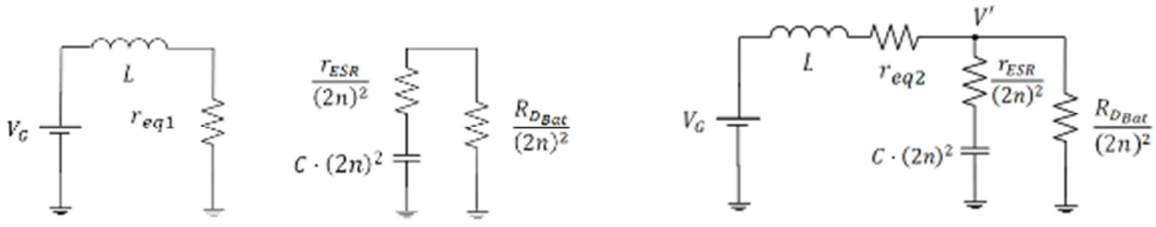
- It is likely that there will be mismatches in switching times of the parallel primary structures of PPIBC. Proper operation of PPIBC is not possible without any means of current balancing.
- All three configurations CBT, PCI and TSI can achieve current balancing.
- CBT is a good solution but it is an extra component in the converter.
- TSI achieves current balancing without an extra component; however it requires two inductors with very close values in order not to have different slopes which is not easy to obtain in practice. In addition double the inductance is required for the same input current ripple compared to single inductor with CBT.
- PCI offers single component acting both as an inductor and current balancing mechanism. Its drawback is that it is a custom solution requiring non-standard coil formers which increases the cost.

3.5 Modeling and Control of PPIBC

One of the topics investigated during this PhD study is dynamic modeling and closed loop control of the PPIBC. A detailed discussion and results are presented in appendix [A3]. A brief introduction to the results will be given in this section.

Target application for PPIBC during this PhD study was a dc-dc converter for a fuel cell stack output. As mentioned in the first chapter, fuel cell output current is expected to have a constant regime in the short term. This requires the PPIBC input current to be the main control parameter; and since it is a boost type topology having its energy storage inductor at the input side, it would be enough to have an average current mode control without any external voltage loop. An important detail on modeling that has been taken into consideration during this research is the load type, which is a battery bank in this case. As explained in [A3], this has changed the dynamic behavior significantly compared to a pure resistive loading for the same power level. Parasitic resistance of the circuit components is another important factor to be considered since it has an effect on the shape of the loop gain as well as the dc gain value.

Based on these criteria, circuit models for both inductor charge and discharge states, as presented in [A3], have been derived and state space equations have been written based on the simplified circuit models as shown in Fig.17. The simplified models have been obtained by reflecting the secondary side impedances to primary side and merging the two parallel full bridge-transformer combinations to a single structure with an effective turns ratio doubled due to the series secondary connection.



(a) (b)

Figure 17 Simplified PPIBC during inductor (a) charging and (b) discharging switching instants

In order to have an accurate model of the complete control loop, a transfer function for the signal conditioning circuit which is an opamp based differential amplifier, has also been derived in order to see especially its phase contribution around the frequencies of interest (~1kHz) which is ~20 degrees. In addition, impedance of the battery bank at the output has been measured and the value around the desired crossover frequency (~1kHz) has been taken.

Using the derived model, a digital controller has been implemented and tested. Fig.18 shows the calculated and measured loop gains matching pretty well with a bandwidth of ~1kHz and a phase margin of ~70 degrees. Fig.19 (a) and (b) shows closed loop operated PPIBC input current soft start and soft stop waveforms, respectively, with a defined ramp of 25A/s. Stable operation with an input current of 50A has been reached from an input source composed of 6 series connected batteries, each of them being 100A/h, to a load battery bank of 5 series connected of the same type.

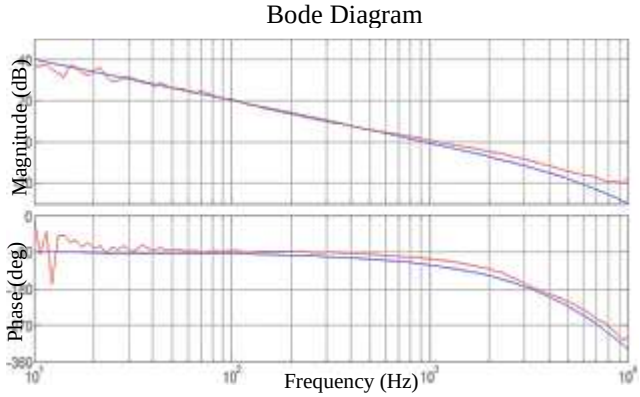
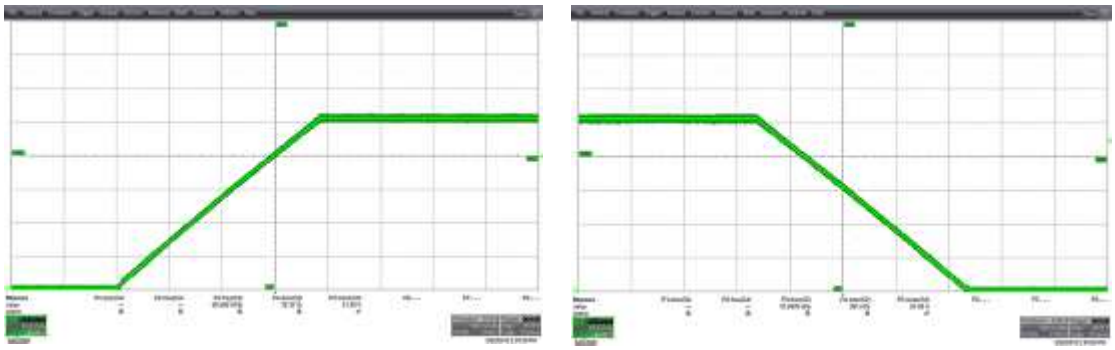


Figure 18 Calculated (blue) and measured (red) loop gains



(a) (b)

Figure 19 (a) Start up and (b) shut down of the input current (10A/div) of PPIBC, time base: 500ms/div

In summary following points can be highlighted regarding the analysis and results obtained in [A3],

- A small signal model of PPIBC with component parasitic elements has been derived with a battery type loading.
- Transfer function of the signal conditioning differential amplifier has also been derived and its gain and phase contribution to the control loop gain has been included.
- Impedance of the load battery bank has been measured with an impedance analyzer and its value around the aimed converter bandwidth has been included in the model.
- A controller designed for a 1kHz bandwidth has been implemented digitally.
- Calculated and measured loop gains have been observed to have a good match.
- Closed loop operated PPIBC has been tested with a soft start and soft stop procedure

3.6 PPIBC with Bidirectional Operation

High current handling capability of PPIBC on the low voltage side makes it very suitable for peak power shaving and regeneration applications especially for electric vehicles where batteries and/or super-capacitors are utilized as secondary storage devices. As part of this PhD project bidirectional operation of PPIBC has been investigated based on the modeling and closed loop control approach explained in the previous section. Experiments have also been carried out with battery banks connected to both sides of PPIBC. Closed loop bidirectional operation of PPIBC has been achieved and a simple start-up procedure has been used based on a digital controller without any external hardware for start-up purposes. PPIBC with bidirectional operation has first been proposed in [A1] and detailed modeling process and experimental results have been presented in [A4], which can be found in appendix. A brief discussion will be included here.

Stable operation of dc-dc converters in closed loop is crucial not only in a single operating point but also in other possible points of steady state operation. In the case of bidirectional dc-dc converters stability becomes even more critical; since generally they are connected to batteries and/or super-capacitors with very high current capability in case of a fault. Consequently an accurate small signal model including non-idealities of the converter has to be used for designing a controller if the same performance is to be expected both from

calculated and implemented designs. It has also been shown in the previous section as well as in [A3] that while converter modeling, using source and load models different from the end application may cause significant differences in gain and phase behavior of the converter bode plot. Also in battery applications, charge and discharge voltage of the battery may change depending on the current. This voltage change may shift the loop crossover frequency since it affects the loop gain. In super-capacitor applications, in order to fully utilize the super-capacitor, its voltage is allowed to vary inside a wide range which also changes the closed loop dynamics similar to the battery case. These increase the importance of accurate converter modeling.

Detailed modeling process of PPIBC is explained in [A4] where a unified model for both current directions is obtained. A DSP based digital PI controller has been designed and the PPIBC has been connected to three Haze HZB-EV12-26 batteries in series on the low voltage side and four in series in the high voltage side. Fig.20 shows the control flow diagram of PPIBC with bidirectional operation. Inductor current is sensed through a Hall Effect sensor with a dc output of 6.25mV/A on top of a 2.5V dc offset. This output is adjusted for the ADC input of the DSP through a differential amplifier. Since a unified model is used for the controller design which is the same for both directions, inductor current direction change is not detected or determined for control purposes. Fig.21 shows the change of current direction from 10A to -10A with a slope of ~80A/s. Converter specifications with frequency domain plots, as well as a soft start procedure for the bidirectional PPIBC in order not to overstress its components, is presented in [A4] which is included in the appendix.

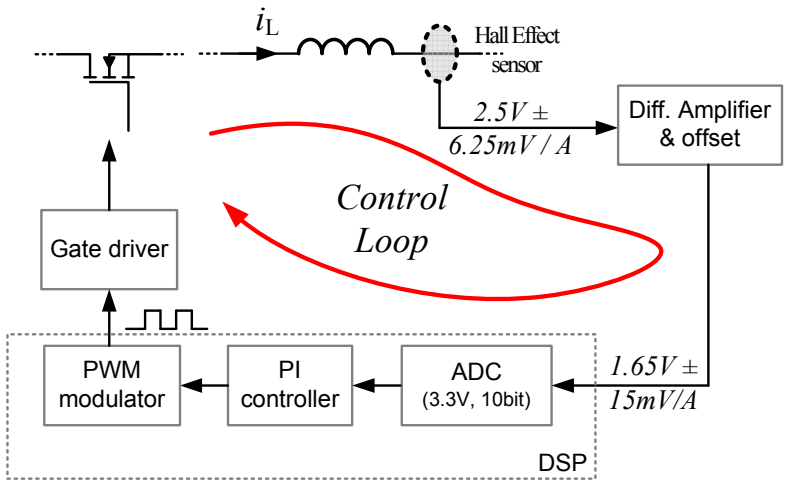


Figure 20 Control diagram of PPIBC with bidirectional operation

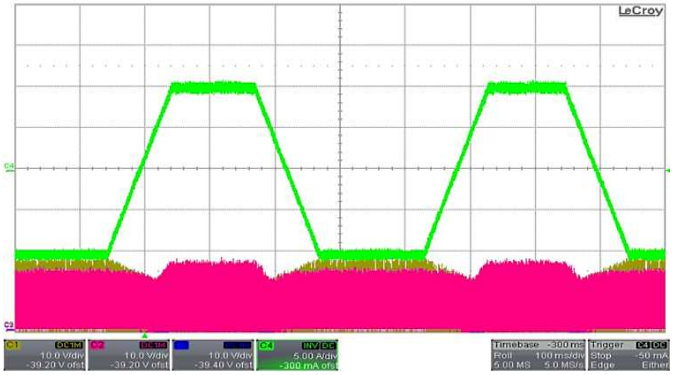


Figure 21 Inductor current direction change with a defined ramp (5A/div. Time scale: 300ms/div)

3.7 PPIBC with Extended Operation Range

One of the disadvantages of isolated boost type dc-dc converters is the 50% theoretical minimum duty cycle for each primary side switch which corresponds to a “no boosting” operating point. Further decreasing the duty cycle is not possible since this will result in a practical “open circuit” situation for the input inductor which can be followed from the simple isolated boost converter circuit in Fig.10. This lower limit for the switch duty cycle also puts a lower limit for the output voltage or an upper limit for the input voltage. One of the drawbacks that this situation causes is the start-up problem of isolated boost converters which is solved by adding an extra winding to the input inductor such that the two windings are coupled. This structure together with a diode can operate similar to a flyback converter and allow the isolated boost converters to extend their operation range below 50% duty cycle for the primary switches. Start-up with flyback winding will be discussed in the next chapter.

Extending the operation voltage range can also be possible by utilizing the multiple primary stages of PPIBC individually as shown in Fig.22 where the discharging state of PPIBC in extended operation mode is given. The details of the extended operation idea is given in [A11] in the form of a paper abstract with simulation and experimental results. As can be observed from Fig.22, primary winding of the transformer T2 is effectively shorted by the two low side switches, S8 and S6, which also shorts its secondary except the leakage inductance. Since only one transformer is active, effective voltage conversion ratio of the converter is halved which is given in Eq. (9).

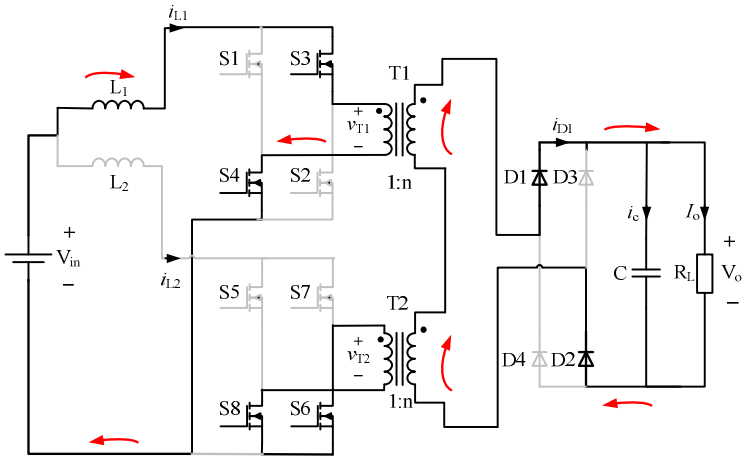


Figure 22 Discharging state of PPIBC with TSI in extended operation mode

$$\frac{V_o}{V_{in}} = \frac{n}{2(1-D)} \tag{9}$$

A disadvantage of the extended voltage range operation is the possible increase in primary switch voltage stress since the output voltage is no more divided in the series secondary windings of the two transformers, T1 and T2. So it can be concluded that this mode is only suitable if there is a large variation in the input and/or output voltages. Another disadvantage is increased leakage inductance per transformer due to the longer secondary path which will cause higher inductive clamp losses in the primary switches for the same input current compared to normal operation of PPIBC. An advantage of the extended operation mode could be simplified transformer design in wide input and output voltage applications where turns ratios has to be selected to cover the whole operation range if only normal operation of PPIBC is preferred.

An important point which needs special attention during the design of closed loop control for PPIBC with extended operation range is the transition between the normal operation and the extended operation. From closed loop stability point of view, the important fact is that the steady state primary switch duty cycle before and after the transition will be different since the effective voltage conversion ratio of the PPIBC will change. This is a step change in duty cycle which will require the control loop to have acceptable phase margin both before and after the transition. A simulated PPIBC transition is shown in Fig.23.

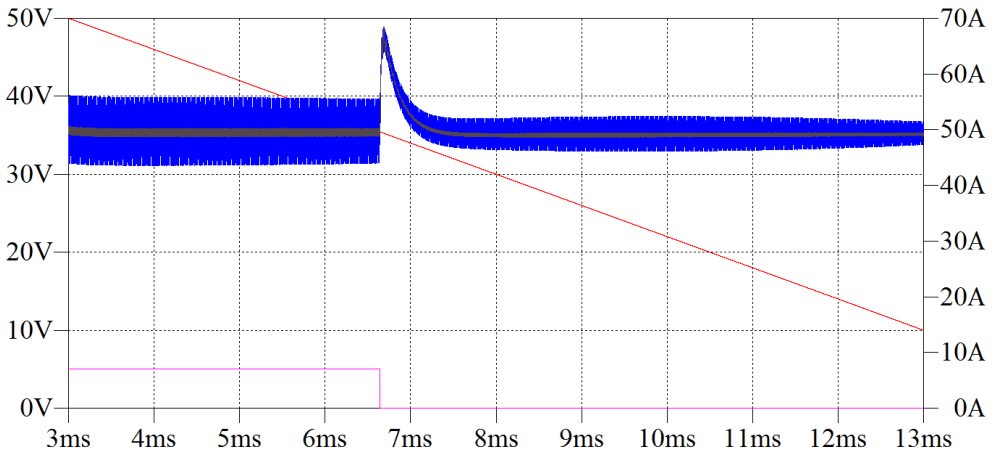


Figure 23 Simulated transition between operating modes: inductor current (I_{L1} + I_{L2}) (blue), filtered input current (dark grey), input voltage in case of a super-capacitor (red) and extended mode control signal (pink).

3.8 Chapter summary

In this chapter firstly, the concept of converter power scaling has been briefly discussed based on [29]. Then primary parallel isolated boost converter (PPIBC) has been introduced with reference to [59]-[61]. Later various topics related to PPIBC have been presented. First, possible current balancing configurations have been analyzed and compared based on [A1] and [A2]. After that, modeling and control of PPIBC based on non-ideal components and battery loading has been introduced referring to the detailed explanations given in [A3]. Next, bidirectional operation of PPIBC, connected to two battery banks at both sides has been discussed based on [A4]. Finally, possibility of extended voltage range operation has been explained referred to [A11].

Chapter IV : Integrated Magnetics for PPIBC

4.1 Introduction

Integration of magnetic components has gained more popularity with time among power electronics designers. Especially planar magnetics with its modular nature allowed different magnetic integration configurations to come out. Recently planar integrated magnetics have been investigated and significant contribution to this area has been made in [62].

Magnetic components based on planar structure have some advantages which make them suitable for switch mode power converters. First of all they have lower profile compared to standard wire-wound magnetic cores. This makes them suitable for compact and high power density design requirements. In addition, their thermal characteristics are better due to the higher surface-to-volume ratio they have. In case of a PCB based planar magnetic design, additional cooling is possible through the planar windings embedded into the main PCB board. PCB based design also brings manufacturing simplicity and cost effectiveness in volume production especially in the case of high current magnetic components where copper foil has to be used instead of copper wire if standard cores are used.

On the other hand planar magnetic technology comes with a number of drawbacks. Wide surface of the planar type cores with the horizontal windings may have a very large footprint. While utilizing the lower profile for a compact design, increased footprint area may not be desirable for every application. Practical limitation of number of turns due to lower copper fill factor is another problem. Especially for PCB based planar windings, significant part of the window area will be filled by the dialectic material. Finally increased inter-winding capacitance can be a problem from common mode noise point of view since planar windings with wider tracks having a longer mean-length-of-turn increases the inter-winding capacitance compared to standard wire wound cores [62]. In this chapter, some planar integrated magnetic solutions for PPIBC which are part of the contribution of this thesis, has been presented. The ideas behind these solutions are utilizing the symmetrical nature of the PPIBC operation, decreasing the required magnetic core volume and number of magnetic components in the circuit. These solutions are explained in detail in the publications in appendix. A brief explanation to each will be given in the following sections.

4.2 Integrated Transformers

Operation of PPIBC was explained in the previous chapter. Symmetrical operation of the parallel primary stages results in the same flux flow in both transformers. In [A5], this feature has been utilized to integrate the two transformers into the same magnetic structure using planar cores and PCB windings as shown in Fig.24. As can be observed from the picture, two planar E core sets are being utilized per transformer sharing a common section in the middle. The overall structure can be obtained by using four E type and two I type planar cores and it has been fixed to the rest of the dc-dc converter circuit with mechanical connectors for easy removal during prototyping. Design details and critical measurements are given in [A5].

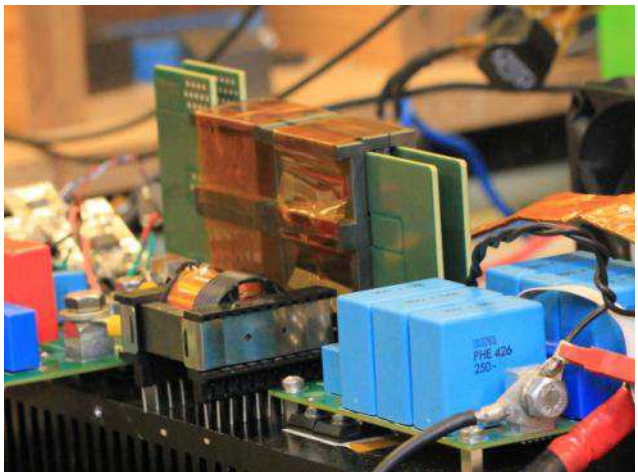


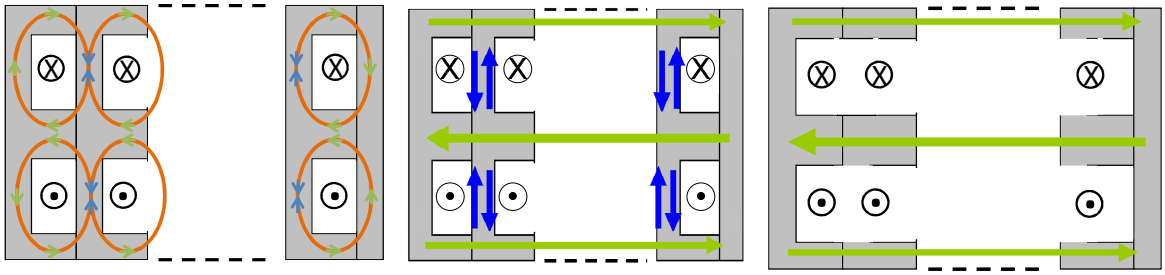
Figure 24 PPIBC with integrated transformers

In this PhD study, integrated transformers are aimed for a nominal 3kW PPIBC module in a fuel cell forklift manufactured by H2Logic A/S. Fuel cell terminal voltage is between 50V to 110V depending on the current drawn and the age. This voltage is to meet the voltage of a battery bank between 65V to 105V depending on the state of charge and the instantaneous current drawn. Converter input current level increases up to 60A at the low end of input voltage range which requires careful selection of copper thickness and winding arrangement in order to keep the conduction losses low. Based on the arguments in [52], substantial interleaving has been used for the 8 layer PCB based windings whose copper thickness is 4 oz. (140um). Ac resistance of each transformer has been measured to be 2.5mΩ at 50 kHz referred to secondary side and 22.5 mΩ referred to primary side. This corresponds to three times its dc value implying an average “m” value between one and two in the Dowell’s ac resistance curve in Fig.7. In order to understand the impact of this to the overall efficiency, ac

resistance of the transformer can be compared to the input impedance of the dc-dc converter as discussed in [29]. In this application input impedance for a nominal input voltage of 70V and a power level of 1.5kW for each parallel primary stage corresponds to 3.267Ω. So the ac resistance of each transformer is approximately 0.7% of the converter input impedance for the nominal operating point, corresponding to the same level of efficiency drop due to transformer conduction losses. However if the converter power is increased to 4kW and the input voltage is decreased to its minimum value of 50V, the impedance ratio becomes 1.8%. This shows the practical power limit of the integrated transformers.

An important feature of the proposed integration method is its modularity as shown in Fig.25 (a), which is suitable for other variations of PPIBC with greater number of parallel primary stages [60]-[61]. As the number of integrated transformers is increased, effective core volume per transformer is decreased which corresponds to less core loss for the same peak-to-peak flux density. Based on the geometrical data provided in [63] for ELP64 planar core, a comparison between an integrated and a separated configuration for a PPIBC with two parallel primary stages shows that 21% less core volume is used and 37% less core volume contributes to the core loss in the case of integration. The reason for further decrease in the core volume contributing to the core loss is due to the flux cancellation as shown with the blue arrows in Fig.25 (b). This implies that for the same operating frequency, peak-to-peak flux density and material, core loss will also decrease with the same amount.

One can argue that since the flux is cancelled in the middle I cores in Fig.25 (b), there may not be any need to keep them as shown in Fig.25 (c). This situation has also been tested during the prototype experiments and the PPIBC with integrated transformers excluding the middle I cores (This means that the two transformers are completely coupled inside the same core structure.) has been observed to be working properly. However, since there may be switching time differences as explained in the previous chapter, the two windings may affect each other in this case of complete coupling, especially if a fault occur in one of the parallel full bridges. In addition, there is a limited window area for each EI or EE planar core sets. In practice this limited area is easily filled up by the PCB windings due to the thickness of the PCB. So the structure proposed in Fig.25 (a) & (b) is more suitable for modularity of PPIBC.



(a) (b) (c)

Figure 25 Conceptual diagram of modular transformer integration (a) individual flux lines for each winding (b) flux cancellation and main flux lines (c) all windings share the same core

4.3 Integrated Current Balancing Transformer

It has been discussed in Chapter 2 of this thesis and [A2] in appendix that some sort of current balancing mechanism is required in order for PPIBC to operate properly. This has been achieved in [59]-[60] with single turn inverse coupled inductors as CBT, which is a separate component in series with the input inductor. The utilization of this component occurs only in a small percentage of the switching period. It acts as high impedance during the switching mismatch moments and behaves like a short circuit during normal switching instants, except its leakage and circuit stray inductance.

In [A6], an integrated inductor and current balancing transformer has been proposed as two circuit elements combined into the same magnetic structure as shown in Fig.26. The winding on the inner leg is part of the input inductor (L) as shown in Fig.27 (a). The two windings on the outer leg stands for the current balancing transformer (Ld) as shown in Fig.27 (b) as well as additional energy storage inductances (Lc) in Fig.27 (a). If the two parallel primary stages have the same switching configuration, current and flux lines occur as in Fig.26 (a). In case of a mismatch, additional flux lines are produced by the differential current flowing from one full bridge to the other as in Fig.26 (b) where the flux lines are flowing inside the high permeability outer portion of the core, resulting in high inductance on the path between the full bridges. Design details and measurements are given in [A6].

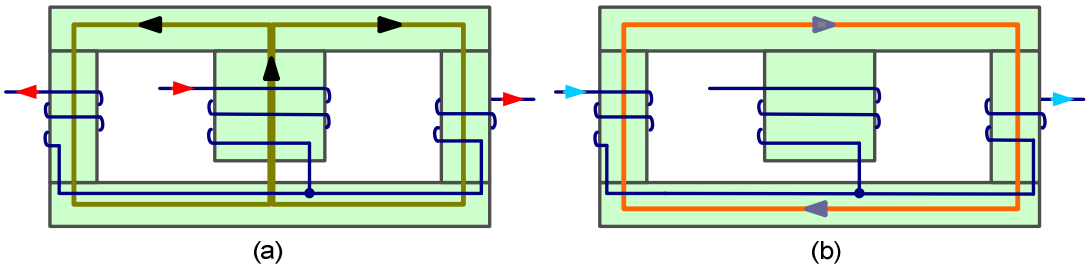


Figure 26 Integrated current balancing transformer current and flux diagram (a) normal operation (b) switching time mismatch moment, resulting in differential current in branches

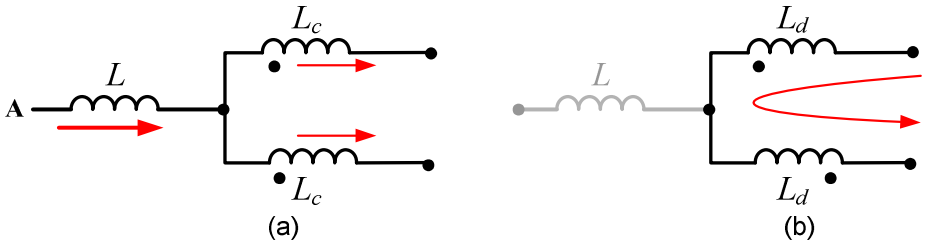


Figure 27 Inductor model (a) normal operation (b) switching time mismatch instant

4.4 Integrated Transformer and Inductor

The magnetic part of PPIBC is composed of transformers, inductor(s) and a magnetic current balancing mechanism. In the previous two sections, integration of transformers and an integrated inductor with a current balancing feature has been presented. In this section a different integration method will be summarized whose details are given in the publications [A7]-[A8] in the appendix.

This integration method is utilizing the modularity of planar magnetics by merging the two transformers and the inductor of a PPIBC into the same E-I-E planar core structure as shown in Fig.28. Similar to the TSI configuration explained in Chapter 2 and [A2], two separate inductors are implemented with air-gaps ground on the center legs of the two planar E cores. The two transformers' primary and secondary windings are wound symmetrically to the side legs of the two E cores. Transformer-inductor pairs for each parallel primary stage are partially decoupled from each other by the middle I core providing a low reluctance path. Provided that the flux pattern of the upper and the lower magnetic structures are the same, complete flux cancellation will occur in majority of the middle I core as shown in Fig.28 (b). Similar to the integrated transformers given in [A5], lower core loss is possible compared to two separate transformer-inductor pairs due to the reduction in effective core volume.

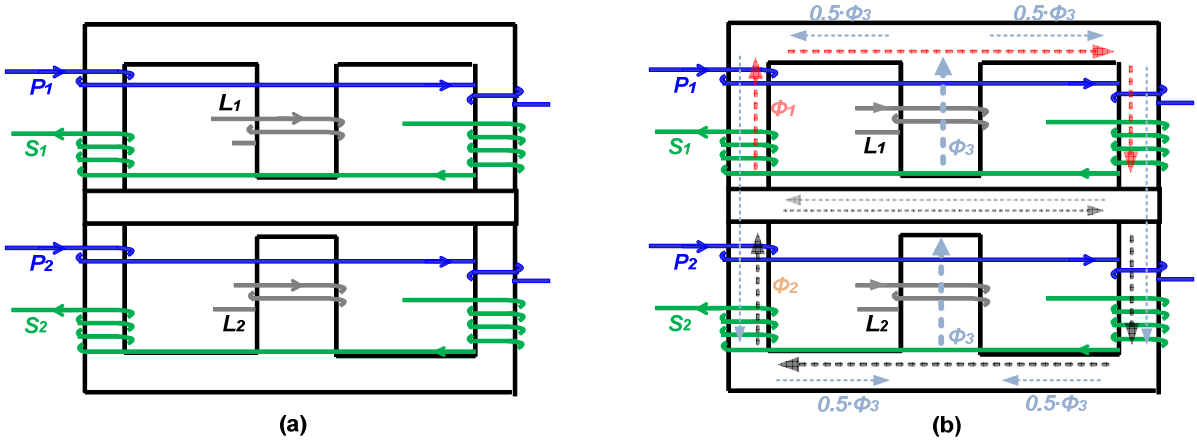


Figure 28 Integrated inductors and transformers for PPIBC,
(a) E-I-E core structure (b) flux distribution

The flux distribution given in Fig.28 (b) shows that the fluxes produced by the inductors and the transformers come on top of each other at different parts of the core having the same, as well as opposite directions. This means that the peak-to-peak flux will not be the same all over the magnetic structure and the core loss as well, which has been shown in the FEA simulations in [A7]. It can be concluded that local saturation points may occur as the power level increases, putting a limitation to the power level of the PPIBC. Another drawback of the structure comes from the current balancing capability point of view. Similar to the current unbalance problem due to different current slopes caused by different inductance values for TSI configuration mentioned in Chapter 2 and [A2], current slopes may deviate from each other especially due to the tolerances in the air-gaps of each E core center leg. An important detail regarding the usage of the middle I core is as follows: In case the middle I core is removed, an undesired situation occurs in terms current balancing since the two inductors becomes directly coupled. This direct coupling turns into an inductance cancellation if a differential current flows from one full bridge to the other as in Fig.26 (b), creating opposing fluxes from each inductor winding. This leaves only the stray inductances in the circuit to oppose the fast current changes between the parallel primary stages in case of switching time mismatches.

4.5 Innovative Start-up of Isolated Boost Converters

A significant drawback of boost type dc-dc converters is the startup and low output voltage case where minimum duty cycle of the switches are no more able to match the input and output voltages, placing the converter voltage and current values in an uncontrollable situation. This problem has been addressed in the literature for isolated boost type dc-dc converters using an extra winding over the input boost inductor. This allows the converter to operate similar to a flyback converter until the output voltage reaches the value which allows the converter to operate in boost mode as shown in Fig.29. However inductor with a flyback winding complicates the manufacturing process increases the price and occupies some part of the available window area, while it is only used for a short time during startup.

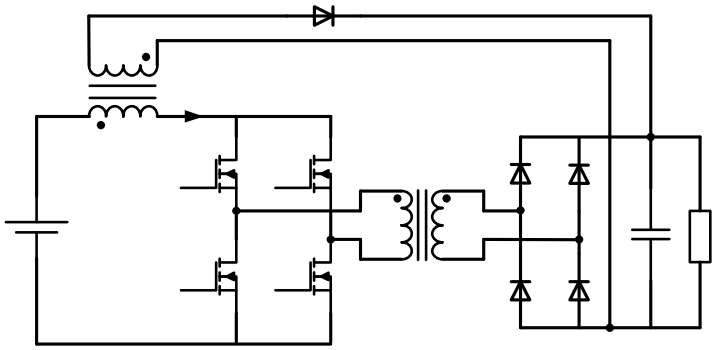


Figure 29 Startup configuration of the simple isolated boost converter with flyback winding

An innovative startup configuration using integrated magnetics is proposed in [A9]-[A10]. The idea is based on integration of inductor and transformer inside the same E-I core structure as shown in Fig.30, which was utilized in the previous section for PPIBC. As explained in [A9], in boost mode of operation of an ordinary isolated boost converter, it is not possible to have a primary switch duty cycle lower than 50% since this will lead to an open circuit for the input inductor, without any means of discharge. Using the innovative integrated start-up configuration, it is possible to have an energy discharge path through the coupling between the inductor winding and the secondary side winding of the transformer. This path is opened when all the switches in the primary side is off. Variations of the integrated startup idea are also applicable to different converter topologies including PPIBC [A10]. Detailed explanation together with the flux diagrams and experimental waveforms are given in [A9].

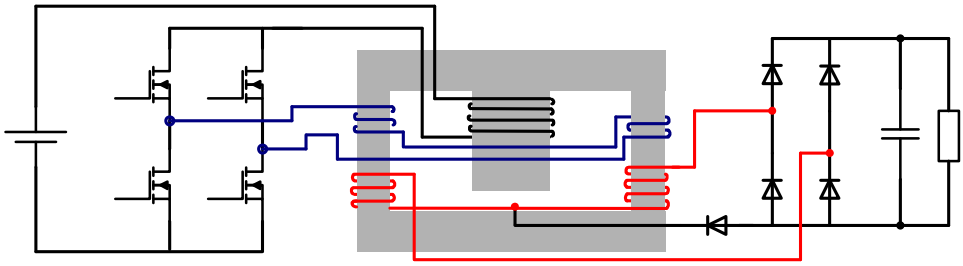


Figure 30 Innovative integrated start-up configuration

One of the drawbacks of the circuit in Fig.30 is its limited power capability similar to Fig.28 compared to discrete component case; because there may be points in the magnetic circuit where inductor and transformer flux add up producing local hot spots in terms of peak flux. In addition the coupling between the inductor winding and the transformer secondary winding is very low. This may result in voltage spikes on the primary switch drain-to-source voltages due to the high leakage inductance caused by the low coupling during the start-up mode. Therefore inductive switching losses during flyback operation will be limiting the efficiency of the converter.

4.6 Chapter Summary

In this chapter, different planar integrated magnetic solutions for PPIBC have been presented. First, planar magnetic technology has been mentioned with its pros and cons. Then a new transformer integration method is presented based on the same flux pattern of PPIBC transformers. Next, an integrated current balancing transformer for PPIBC is proposed reducing the number of components by adding a current balancing capability to the input inductor. Later, integration of magnetics is further extended to inductor and the transformers by utilizing the modular planar magnetic cores and PCB windings. Finally an innovative startup configuration is presented for isolated boost type dc-dc converters.

Chapter V : Conclusions and Future Work

5.1 Summary and Conclusions

In this work various topics are presented related to analysis and design of primary parallel isolated boost converter (PPIBC) which is a simple and promising dc-dc converter topology regarding its efficient high current carrying capability.

The thesis starts with a brief explanation of fuel cells and batteries which are commonly employed together with dc-dc converters in renewable energy and electric power based transportation applications. Possible configurations for interfacing fuel cell stacks with secondary energy storage devices and dc-dc converters are also mentioned.

In many applications, efficient power processing is one of the main goals when designing dc-dc converters; and efficient dc-dc converters can be obtained by paying attention to several factors such as topology selection, magnetic component design and power stage layout. As part of this thesis these factors are summarized based on [29].

In Chapter 2, topics including current balancing, closed loop control, bidirectional operation and extended voltage range operation are presented with detailed explanations given in corresponding publications. The main points of this research related to these topics can be summarized as follows:

- Parallel primary stages of PPIBC may have differences in their switching times due to many reasons such as component and layout tolerances. This is the reason of using a current balancing transformer (CBT) which is a simple magnetic structure; however it is an additional component in the circuit in series with the input inductor. It is also possible to achieve current balancing by using two separate inductors (TSI), one for each primary parallel stage. The drawback of this approach is the inductance tolerances of the inductors which causes another source of current imbalance due to the differences in the two current slopes. Partial coupling (PCI) method combines current balancing and energy storage into the same component with the drawback of necessity for a non-standard coil former.

- Detailed dynamic model of PPIBC is derived including the component parasitic resistances, load type as a battery bank, signal conditioning amplifier transfer function and calculation delay of the digital control algorithm. It has been observed that battery as a load results in a different converter gain and phase plot compared to a pure resistive loading for the same power level which is generally preferred for modeling of dc-dc converters. It is also observed that it is possible to have a good match between calculated and measured loop gains of PPIBC if the control loop is modeled correctly including non-idealities. An important detail regarding the battery as a load is its internal (frequency, state-of-charge, state-of-health dependent) impedance and current dependent terminal voltage which changes the control loop gain.
- Bidirectional operation of PPIBC is studied and a digital controller based prototype is implemented and tested with battery banks connected to both sides. A unified dynamic model is derived for both directions of operation. It has been observed during experiments that a proper soft start procedure is required in order to prevent voltage and current stress over the components. This has been implemented by progressive adjustment of the current reference and sequential introduction of synchronous rectification.
- An idea for extending the operation voltage range of PPIBC is proposed based on deactivating one of the parallel primary stages. Using this new idea, it is possible to change the voltage conversion ratio of PPIBC such that lower output voltage and/or higher input voltages can be covered. The drawback of the method is increased leakage inductance and primary switch voltage stress. Special attention is needed for the transition between normal operation and extended operation modes since the steady state conditions of the converter change.

In Chapter 3, a number of planar integrated magnetic solutions for PPIBC are presented. These solutions utilize the symmetrical structure of PPIBC where the parallel modules work synchronously. The prototypes built during this research are based on PCB windings in order to provide simple manufacturing alternatives for magnetic components. The achievements of this research in terms of PCB based planar integrated magnetics is summarized below:

- A transformer integration approach for PPIBC is proposed which offers a modular PCB based implementation. Due to the operation symmetry of the transformers, flux cancellation occurs in certain parts of the core structure which reduces the core loss. Compared to a discrete transformer solution with the same core type, integrated transformers require less core volume.
- An integrated current balancing transformer is proposed where input inductor and current balancing transformer are merged into the same core structure, reducing the number of components in PPIBC as well as the total volume of the magnetic cores. Also the extra windings wound on the side legs are coupled in a way that they appear as additional inductance to the input inductor.
- Transformers and inductor(s) of PPIBC are integrated based on E-I-E planar cores with the inductor placed in the center leg with an air-gap and transformer windings are placed in the side legs. Flux cancellation occurs in certain parts of the middle I core which reduces the core loss and volume compared to a PPIBC with discrete magnetic components.
- E-I-E integration is further manipulated resulting in an innovative start-up configuration for isolated boost type dc-dc converters where secondary winding(s) can be used similar to a flyback winding which utilizes the coupling to the integrated input inductor. This solves the start-up problem of the isolated boost type converters avoiding the added complexity to the input inductor with an extra flyback winding.

5.2 Future Work

- Different current balancing strategies preferably not using magnetic components can be investigated.
- Based on the derived dynamic model obtained, advanced control strategies can be applied in order to ensure that the PPIBC shows a satisfactory performance in variable voltage applications such fuel cells and batteries.
- PPIBC with bidirectional operation can be applied to super-capacitor based regenerative braking applications where high currents are to be handled.
- PPIBC with extended voltage operation range can be implemented and mode transition without any component overstress can be verified.

- Planar PCB windings and temperature rise relationship can be investigated in order to see the power limits of a parallel module for PPIBC in a certain application.

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Appendix A

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Appendix A1

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Isolated Bidirectional DC–DC Converter for SuperCapacitor Applications

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Abstract. This paper proposes a new bidirectional DC/DC converter for supercapacitor applications. The proposed converter has a parallel structure in supercapacitor side (where voltage is low and current is high) and a series structure in the other side. This structure increases efficiency of the converter. For current sharing in the parallel side of the proposed converter, two different methods are recommended and compared in this paper: Current balancing transformer (CBT) and two separate inductors (TSI). Simulation and experimental results show performance of the proposed converter.

Key words

Current sharing, parallel primary, bidirectional converter, supercapacitor, fuel cell.

1. Introduction

Currently fuel cell electric vehicles (FCEV) are considered as an attractive option for future cars because of environmental issues and alternative energy requirements. However since fuel cell stack has a slow response, using an auxiliary energy storage device such as battery or supercapacitor (SC) is recommended in the fuel cell (FC) applications [1-3]. While the battery has a large energy density and SC has a high power density, FC-Battery hybrid and FC-SC hybrid systems offer different features. However, FC-SC-Battery hybrid systems in Fig. 1 have been shown to have superior features [2-3].

Because of charge dependent voltage of SC, a bidirectional DC/DC converter is needed for bidirectional power exchange between SC and other parts of the system for different voltage levels [2-4]. Isolated full-bridge converter in Fig. 2 is a common DC/DC converter topology [5-6]. For high power applications, parallel isolated full-bridge converters have been proposed [7]. In fuel cell applications, generally low voltage is required to be boosted to higher voltages. Fig. 3 shows the primary parallel isolated boost converter proposed in [8] which is suitable for high voltage gain applications. This converter is composed of full-bridge stages with parallel primary connections (where current is high and voltage is low) and a single rectification stage with series secondary connection (where current is low and voltage is high). Current sharing is ensured by the series connection of transformer secondary windings and small cascaded current balancing transformer (CBT) on the primary side.

In this paper, the unidirectional converter presented in [8] is modified to handle bidirectional power flow in energy storage applications. For this purpose, the diode bridge rectifier on the secondary side has been replaced with a full bride inverter. In addition a detailed analysis has been carried out comparing two different current balancing configurations. Using two separate inductors (TSI) instead of current balancing transformer (CBT) is recommended due to cost and simplicity. It has been shown that the current sharing performance is similar in both cases.

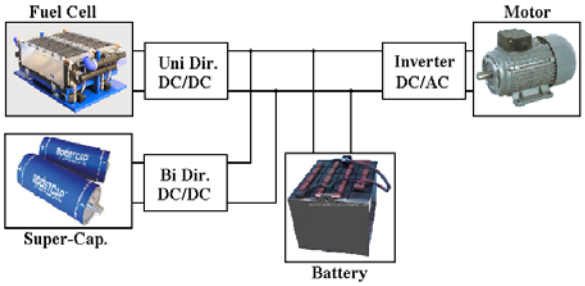

Fig. 1. FC-SC-Battery hybrid system.

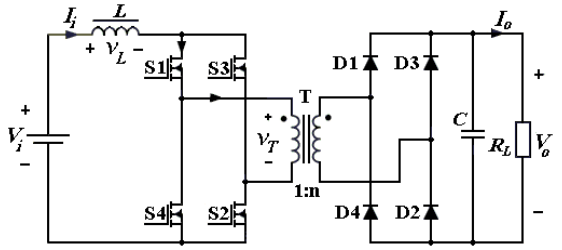

Fig. 2. Isolated full-bridge DC/DC converter.

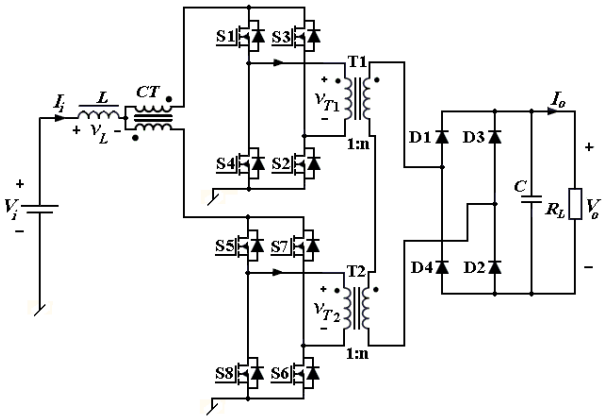

Fig. 3. High-efficiency isolated DC/DC converter.

2. Bi-directional DC/DC Converter

Fig. 4 shows the modified bidirectional DC/DC converter suitable for SC applications. The converter includes two full-bridge stages in the primary side and one in the secondary. Two inductors with the same value (L_1=L_2) are used as boosting elements. This configuration (TSI) can eliminate the requirement of current balancing transformer (CBT). The proposed converter has two discharging and charging operating states. These states will be illustrated in the following sections.

Fig. 5 shows the gate signals for the proposed converter. The gate signals for the primary side switches are similar to the original unidirectional configuration. The gate signals for the secondary side can be produced using the logical NOT of the gate signals of primary side switches. However to avoid short-circuit in the output, dead-time should be considered.

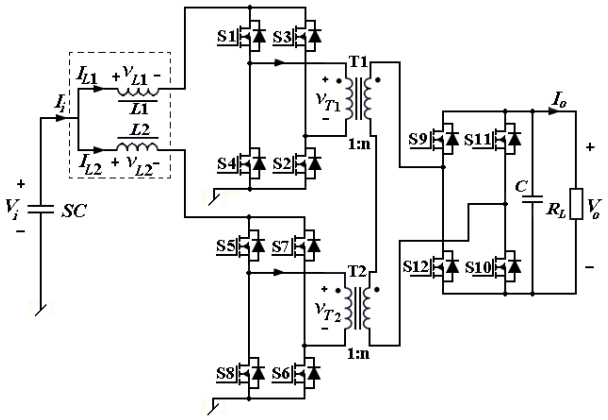

Fig. 4. Proposed isolated bi-directional DC/DC converter.

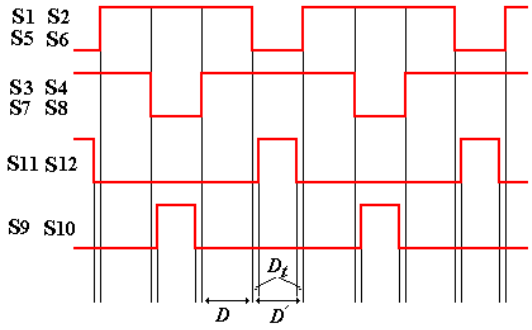

Fig. 5. Gate signals of proposed converters.

3. Normal Operation Modes

The proposed converter can be simply modeled as in Fig. 6a and Fig. 6b for CBT and TSI configurations, respectively. Upper and lower primary full-bridge stages have been modeled by switches S_{m1} and S_{m2} and secondary side bridge has been modeled by S_m.

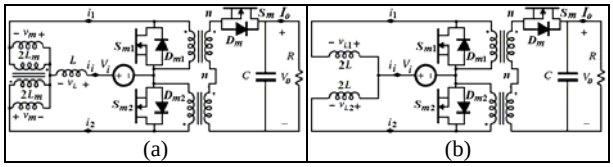

Fig. 6. Simplified models of the proposed conveteter: a) CBT b) TSI.

A. *Discharge state*

In the discharging of SC, secondary inverter acts as a rectifier. Considering the gate signals in Fig. 5, two main operation modes can be defined for the converter.

1) Mode 1: Both S_{M1} and S_{M2} are closed and inductors are charging (Fig. 7).

2) Mode 2: Both S_{M1} and S_{M2} are open and inductors are discharging (Fig. 8).

Fig. 9 shows waveforms for both inductor configurations. For the same ripple current, inductance of each inductors of TSI topology is twice of inductance of inductor of CBT topology. It can be proven for both cases that:

$$V_o = \frac{2n}{D'} V_i \quad (1)$$

$$I_i = \frac{2n}{D'} I_o \quad (2)$$

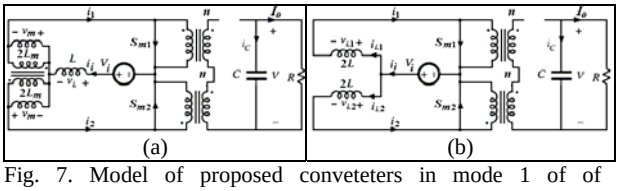

Fig. 7. Model of proposed conveteters in mode 1 of of discharging state: a) CBT b) TSI.

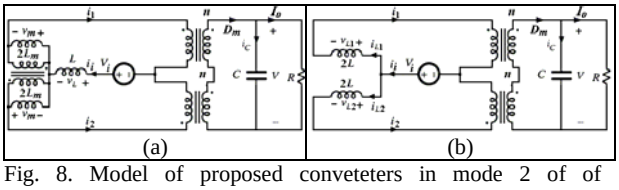

Fig. 8. Model of proposed conveteters in mode 2 of of discharging state: a) CBT b) TSI.

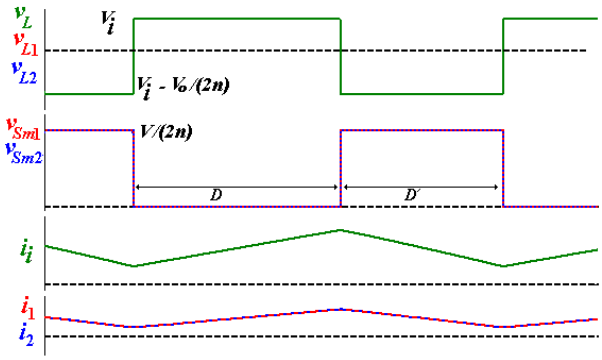

Fig. 9. Waveforms of proposed converters in normal modes of discharging state.

B. Charge state

Primary side full-bridge stages act as rectifiers during the charging of the SC. Similar to the discharge state, two main operation modes can be considered in the charge state.

1) Mode 1**:** Both diodes D_{M1} and D_{M2} are conducting and inductors (or inductor) are discharging (Fig. 10).

2) Mode 2: Both D_{M1} and D_{M2} are open and inductors (or inductor) are charging (Fig. 11).

Fig. 12 shows waveforms for both configurations. Neglecting deadtime, it can be proved that (1) and (2) are correct in the charge state. However considering deadtime (Fig. 5), it can be written:

$$V_o = \frac{2n}{D' - 2D_t} V_i \quad (3)$$

$$I_i = \frac{2n}{D' - 2D_t} I_o \quad (4)$$

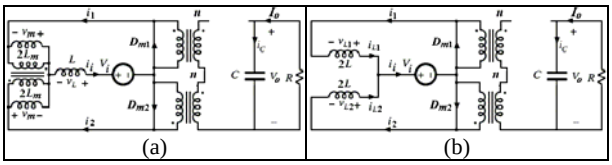

Fig. 10. Model of proposed conveteters in mode 1 of of charging state: a) CBT b) TSI.

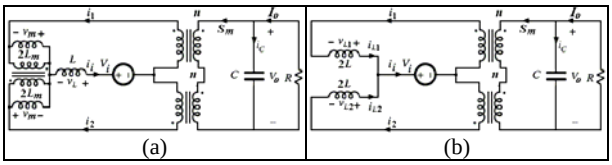

Fig. 11. Model of proposed conveteters in mode 2 of of charging state: a) CBT b) TSI.

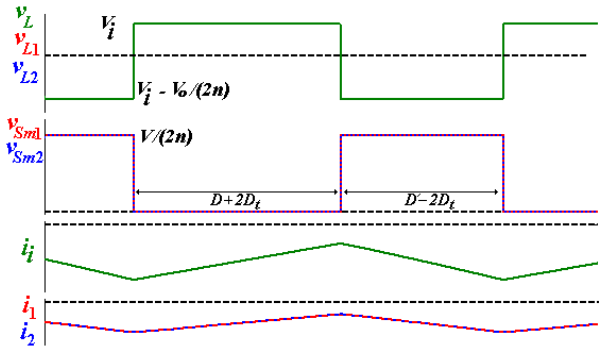

Fig. 12. Waveforms of proposed converters in normal modes of charging state.

4. Extra Operation Modes

In the previous section, it is assumed that both primary side switches are switched at same time. However it is possible that this assumption is not satisfied because of differences in component propagation delays and parasitic elements. Considering a single boosting inductor (without CBT), when one of the simplified switches in Fig. 6 is ON, all the current i_i passes through the corresponding bridge. However in CBT and TSI configurations, due to the high impedance seen between the two full-bridge structures, the current going through each full-bridge can not change instantaneously. Therefore either CBT or TSI should be included in the topology for proper current balancing.

A. Discharge state

*T*wo extra modes can be defined in discharge state:

1) Mode 3 (Fig. 13): S_{M1} is ON and S_{M2} is OFF. When both modeling switches S_{M1} and S_{M2} are OFF, but $i_2 > i_1$, this mode also can be created as diode D_{M1} is ON.

2) Mode 4 (Fig. 14): S_{M1} is OFF and S_{M2} is ON. When both modeling switches S_{M1} and S_{M2} are OFF, but $i_1>i_2$, this mode also can be created as diode D_{M2} is ON.

Extra modes 3 and 4 are generally similar to mode 2; however currents i_1 and i_2 are not equal in these modes. As an example, assuming a delay for turning S_{M1} ON, we will investigate the operation of the converter in both CBT and TSI configurations.

1) CBT: When both switches S_{M1} and S_{M2} are OFF, converter is in mode 2. When S_{M1} turns ON and S_{M2} is OFF (due to signaling mismatch), converter has mode 3 (Fig. 13-a). In this mode CBT sees a non-zero voltage; therefore magnetizing current of CBT is increasing. This current creates a current difference between two primary inverters. With turning S_{M2} ON, converter goes to mode 1, while there is a constant current difference between two primary bridges. When both switches turn OFF again (it is assumed no delay for turning OFF), converter can not enter to mode 2 because inverter currents are not same. Since i_1 is greater than i_2, simplified diode D_{M2} is forced to be ON and thus converter will be in mode 4. During mode 4, CBT sees negative non-zero voltage and magnetizing current of CBT is decreasing. Mode 4 continues until both inverter currents are the same. The required time interval for this is equal to the switching delay time interval between the two switches, S_{M1} and S_{M2}. After mode 4, converter goes to mode 2. Fig. 15-a shows the waveforms of CBT topology in this condition.

2) TSI: When both switches S_{M1} and S_{M2} are OFF, converter is in mode 2. When S_{M1} turns ON and S_{M2} are OFF (due to signaling mismatch), converter is in mode 3 (Fig. 13-b). In this mode inductors see different voltages; L_1 sees positive voltage and L_2 sees negative voltage. This creates a current difference between the two inductors. With S_{M2} turning ON, converter goes to mode 1, while there is a constant current difference between the two primary bridges. When both turn OFF again, converter can not enter to mode 2 because inverter currents are not same. Since i_1 is greater than i_2, simplified diode D_{M2} is forced to be ON and thus converter will be in mode 4. During mode 4, L_1 sees negative voltage and L_2 sees positive voltage. Therefore the current difference between the inductors is decreasing. Mode 4 continues until both bridge currents are the same. The required time interval for this is equal to the switching delay time interval between the two switches, S_{M1} and S_{M2}. After mode 4, converter goes to mode 2. Fig. 15-b shows the waveforms of TSI topology in this condition. For both configurations, it can be proven that:

$$V_o = \frac{2n}{D' + d_{on}} V_i \tag{5}$$

$$I_i = \frac{2n}{D' + d_{on}} I_o \tag{6}$$

For both configurations, it can be seen from Fig. 15 that average of currents i_1 and i_2 are not equaled when there is a switching delay. Defining current difference I_d as:

$$I_d = 0.5(I_1 - I_2) \tag{7}$$

Therefore for CBT and TSI configurations it can be written that:

$$I_{d-CBT} = \frac{D\, d_{on} V_i}{2\, f_{SW} L_m (D' + d_{on})} \tag{8}$$

$$I_{d-TSI} = \frac{D\, d_{on} V_i}{2\, f_{SW} L (D' + d_{on})} \tag{9}$$

Therefore for $L=L_m$, both configurations have similar current difference. However assuming d_{on} is small, current difference (I_d) is small in both configurations.

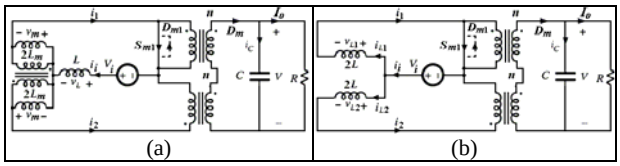

Fig. 13. Model of proposed conveteters in mode 3 of of discharging state: a) CBT b) TSI.

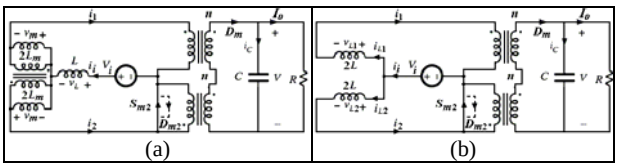

Fig. 14. Model of proposed conveteters in mode 4 of of discharging state: a) CBT b) TSI.

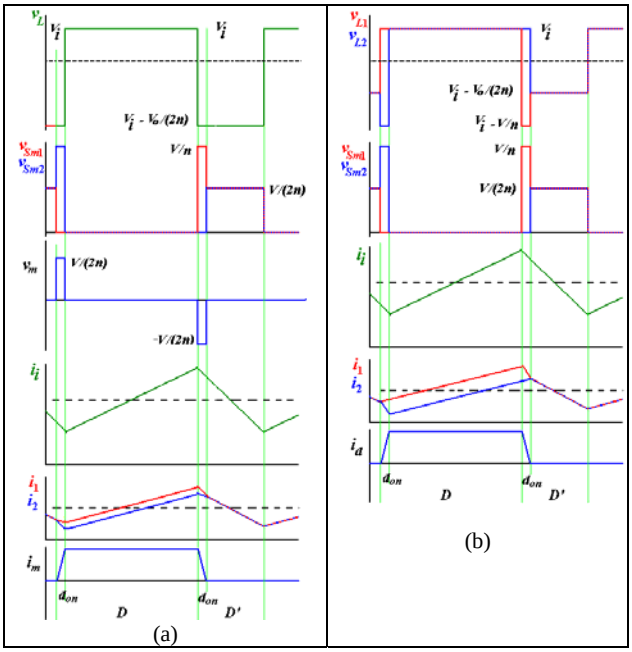

Fig. 15. Waveforms of proposed converters in discharging state with switching delay.

B. Charge state

Similar to discharge state, two extra modes can be defined for charge state:

1) Mode 3 (Fig. 16): D_{M1} (or S_{M1}) is ON and D_{M2} is OFF.

2) Mode 4 (Fig. 17): D_{M1} is OFF and D_{M2} (or S_{M2}) is ON.

Similar to discharge state, extra modes 3 and 4 are generally similar to mode 2; however currents i_1 and i_2 are not equal in these modes. In charge state, if switching delays are smaller than the deadtime, extra modes does not occur. However, extra modes can occur due to the difference between inductor values.

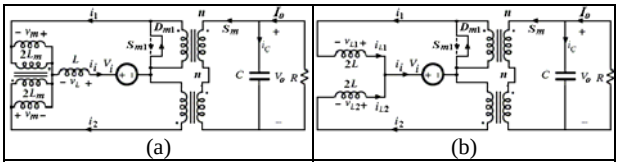

Fig. 16. Model of proposed conveteters in mode 3 of of charging state: a) CBT b) TSI.

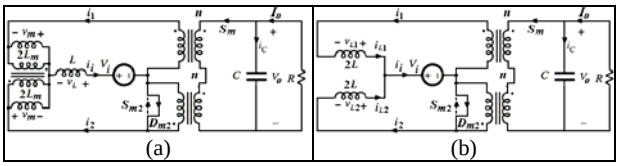

Fig. 17. Model of proposed conveteters in mode 4 of of charging state: a) CBT b) TSI.

5. Control System

A hybrid system such as in Fig. 1 usually includes a central control system (CCS) and several local control subsystems (Fig. 17-18). Regarding system condition, CCS determines references signals for the control subsystems.

In this paper, it is assumed that the reference current of SC is determined by CCS. Fig. 19 shows the control subsystem for the proposed converter for an SC application. Control system is based on average current mode control. A PI controller has been used for ensuring the steady state current error to be zero. Output of PI is a duty cycle value that it is applied to the PWM block.

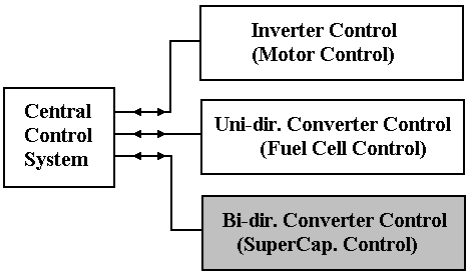

Fig. 17. Control system of FC-SC-Battery hybrid system (Fig. 1).

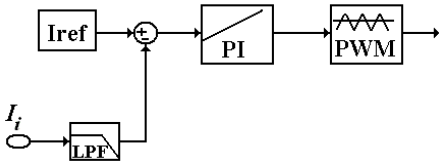

Fig. 18. Control subsystem of proposed bidirectional converter (supercapacitor).

6. Simulation and Experiments

To verify the proposed converter, the control system shown in Fig. 18 was used for simulation. Table 1 shows simulation parameters. A step signal has been used as the reference current; it changes from -100A to 100A at t=2ms. Before t=2ms the converter will be in the charge state and after that converter should go to the discharge state. Simulation results have been shown in Fig. 19. It can be seen that the SC current (I_i) is able to track the reference current signal in both charge and discharge states.

An experimental prototype of the modified bidirectional DC-DC converter was also built using digital signal possessor (DSP) control (Fig. 20). Experimental current I_i has been shown in Fig. 21. It could be observed that that the closed loop controller implemented in the DSP is able make the SC current follow the reference current in a stable manner. Implementation of the two transformers with primary parallel and secondary series connection is realized with planar E-type cores.

Table I. - Simulation Parameters

Parameters	Values
Capacitance of SC	100 F
Internal resistance of SC	0.005
Initial voltage of SC	25 V
Battery voltage (V_o)	80 V
Proportional gain (Kp) of PI	0.001
Integral gain (Ki) of PI	10
Transformer turns ratio (n)	3
Inductors	10 uH
Switching Frequency	50 kHZ

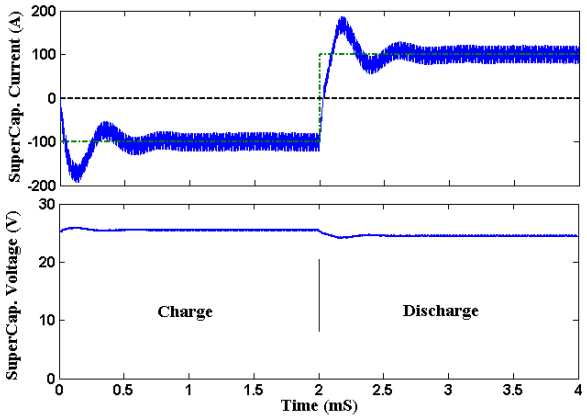

Fig. 19. Simulation results: Current and voltage of supercapacitor.

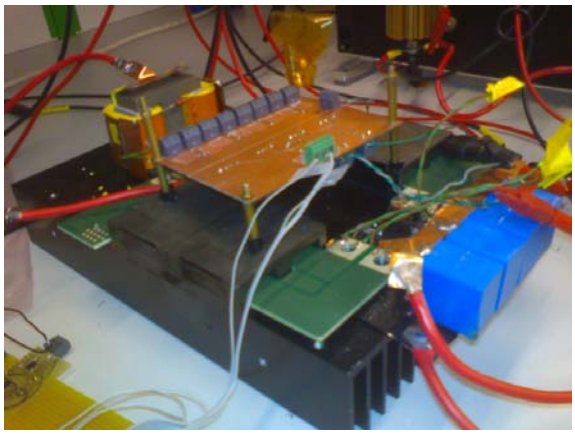

Fig. 20. Experimental prototype of the proposed converter.

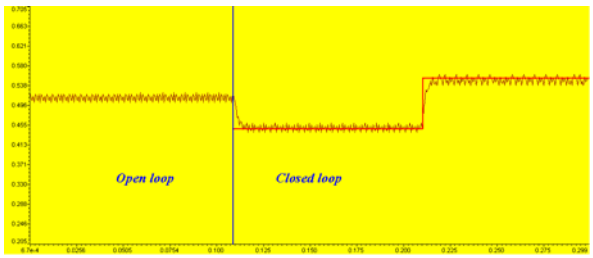

Fig. 21. Experimental results:Reference and (filtered) actual current (sampled by the DSP).

7. Conclusion

In this paper an isolated bidirectional DC/DC converter has been proposed for supercapacitor applications. The proposed converter uses a parallel structure on the primary side (low-voltage high-current side) and a series structure in secondary side (high-voltage low-current side). This structure has already been used for unidirectional power flow in the literature. It has been developed for bidirectional power flow in this paper. Also a new method was proposed for current sharing on the primary side. In the proposed method, separate inductors can be used instead of the conventional method which is based on a current balancing transformer. Although both methods have almost the same performance, manufacturing the separate inductors is easier. However, inductance value tolerances can be a problem in fair current distribution between the parallel primary stages. Performance and validity of the proposed converter has been verified by simulation and experimental results.

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Appendix A2

[A2] **G. Sen**, S. M. Dehghan, O. C. Thomsen, M. A. E. Andersen, L. Møller, "Comparison of current balancing configurations for primary parallel isolated boost converter," in Proc. ACEMP, Istanbul, Turkey, 2011 (**Published**).

Comparison of Current Balancing Configurations for Primary Parallel Isolated Boost Converter

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***Abstract*— Different current balancing configurations have been investigated for Primary Parallel Isolated Boost Converter (PPIBC). It has been shown that parallel branch current balancing is possible with several configurations of coupled/uncoupled inductors. Analytical expressions for branch currents have been derived for different cases of gate signal mismatch causing current imbalance. It has been observed that turn-on and turn-off delays in parallel power stages of the PPIBC have different effects in the branch currents deviating from ideal. It has also been observed that in some configurations inductance differences due to core tolerances play an important role in current imbalance. Analytical and simulation results have shown that another side effect of the gate signal delay and inductor value difference is additional voltage stress over the switches during the mismatch times. Advantages of each configuration in terms of effective current balancing, efficiency and manufacturing simplicity have been highlighted. Simulations with ideal components for each case have been carried out to confirm the analytical derivations. Experimental results have also been included to show the performances of different configurations where component non-idealities like transformer leakage inductances also become effective.**

I. INTRODUCTION

Primary Parallel Isolated Boost Converter (PPIBC) is a high efficient topology for high input current, step up applications [1]. The effectiveness of the topology is coming from the unique parallel power stage structure in the input side where the voltage is low and the current is high. The primary side switches of each parallel power stage operate synchronously with the corresponding switches in the other parallel power stages. However due to propagation delays and rise-fall time differences of the ICs as well as component tolerances in the gate drive circuitry like gate resistances result in switching delays. These delays not only cause the branch current values to deviate but also switch voltage over-stress conditions to occur which may increase the switching losses.

Although various configurations have been claimed in the patent [2], only one of them, current balancing transformer (CBT), has been implemented so far for proof of concept. Recently integrated magnetic solutions have been proposed for this topology [3] and [4]. Deviations from ideal current waveforms in parallel branches have been reported in [5]. Similar effects can be observed if two separate inductors (TSI) or partially coupled inductors (PCI) are used. In this paper these configurations have been analytically investigated. Expressions have been derived for branch current deviations which then compared to ideal circuit simulation as well as experimental results.

II. PRIMARY PARALLEL ISOLATED BOOST CONVERTER

Fig.1 shows PPIBC topology suitable for handling high input currents for fuel cell applications. The current is forced to be equal in both primary windings by the series secondary connection of the two transformers. Primary switches share the same control signals with the same phase switching sequence which allows a simple control. Output rectification unit as well as input and output filters are common to both primary stages.

The input inductor in Fig. 1 serves as an energy storage element for both primary power stages. As long as switches S1, S2, S3, S4 and S5, S6, S7, S8 work in the same pattern (Fig. 2a), the inductor current will be shared equally by the two full bridges. In case of a mismatch in switching, the CBT (effectively an inverse coupled inductor) in series with the input inductor shows high impedance in the differential path which limits the rate of change of the differential current (Fig. 2b).

III. CURRENT BALANCING CONFIGURATIONS

In order to simplify the analysis, the converter in Fig. 1 has been reduced to the circuit in Fig. 3a. This circuit will be used through out the paper except the coupled/uncoupled inductor combinations will replace the single inductor.

A. Single inductor:

Figs. 3b-e show possible configurations of the switches both in normal and extra operation modes. Here a switch being on is equal to all four switches being on (inductor charging state). Similarly a switch being off in Fig. 3a corresponds to two diagonal switches being on in Fig. 1 (discharging state).

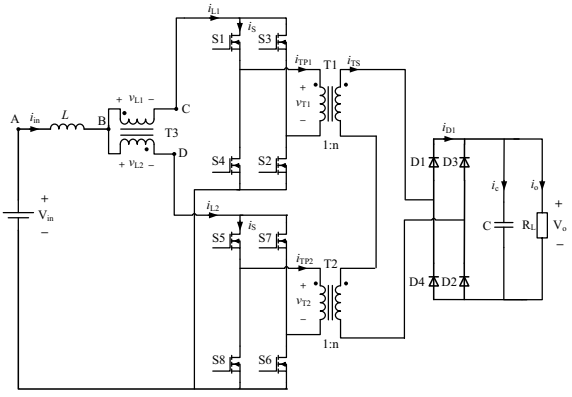


Fig. 1. PPIBC with coupled inductors for current balancing

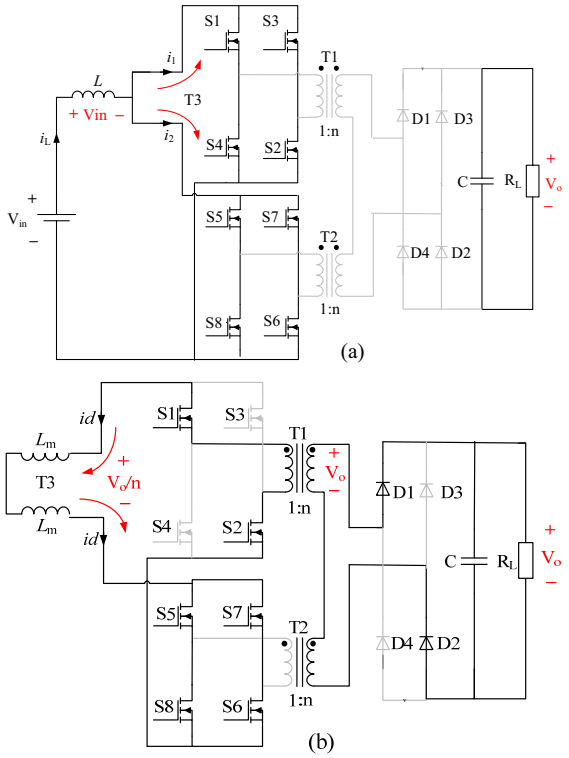
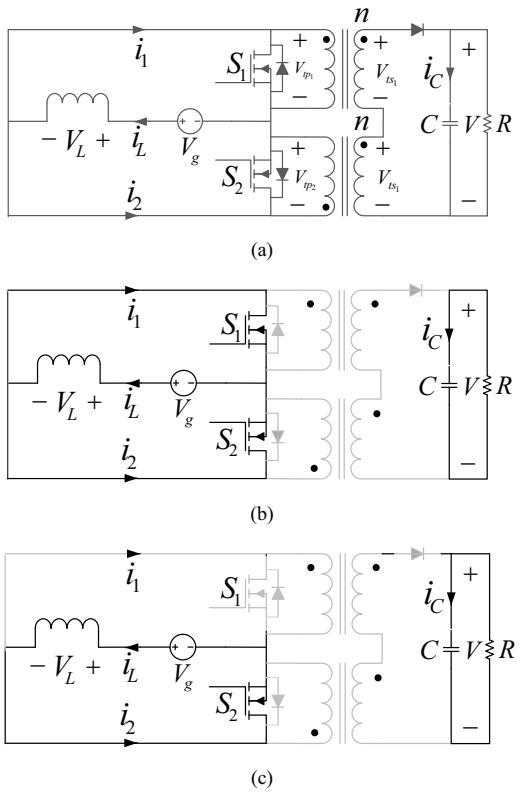


Fig. 2. (a) Forward current path in both branches during boosting (b) differential current path during gate signal mismatch

As can be observed from the branch current waveforms in Fig. 4, significant deviations occur from ideal situation at the times of turn off and turn on delays. All the input current is directed to the branch where the switch is on.



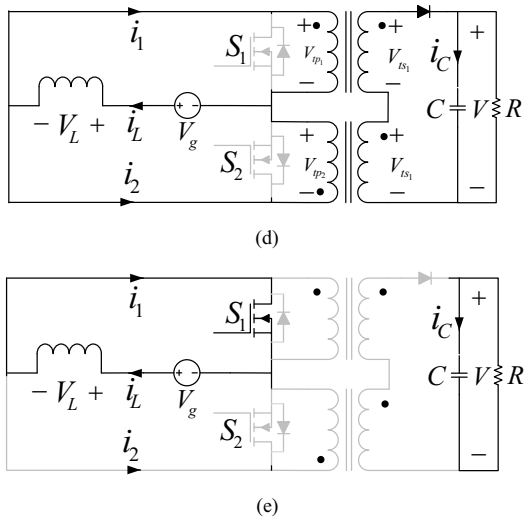


Fig. 3. (a) Simplified PPIBC with a single inductor (b) charging period (c) turn off delay in S_2 (d) discharging period (e) turn on delay in S_2 (inactive lines and components have been drawn light grey)

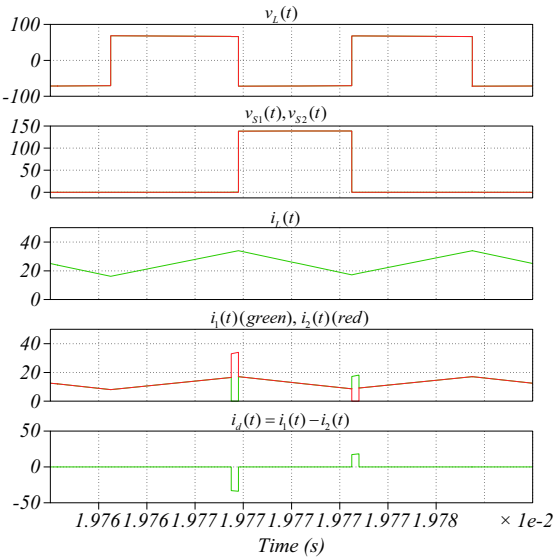


Fig. 4. Simulated waveforms of single inductor case

Relative switching delays also changes the steady state operating point of the converter by changing the effective duty cycle. Assuming that there is both a turn off and turn on delay in S_2, following expressions can be obtained:

$$(D+d_{off})(V_g)+(D'-d_{off})(V_g-V/(2n))=0 \quad (1)$$

$$V=\frac{2n}{D'-d_{off}}V_g \quad (2)$$

$$(D+d_{off})(-V/R)+(D'-d_{off})(I_L/(2n)-V/R)=0 \quad (3)$$

$$I_L=\frac{2n}{D'+d_{off}}\frac{V}{R} \quad (4)$$

Average branch current expressions can be derived from here:

$$I_1=I_L/2+K \qquad I_2=I_L/2-K \quad (5)$$

where,

$$K = d_{on}[I_L - (D + d_{off} - d_{on})V_g/(2 f_{SW} L)]/2 - d_{off}[I_L + (D)V_g/(2 f_{SW} L)]/2 \quad (6)$$

In these equations, d_{on} and d_{off} represent the turn on and turn off delay, respectively. Similar situation occurs if two direct coupled inductors are used instead of a single inductor as seen in Fig. 5. This configuration has the same waveforms as in Fig. 4. Consequently both configurations have poor current balancing features.

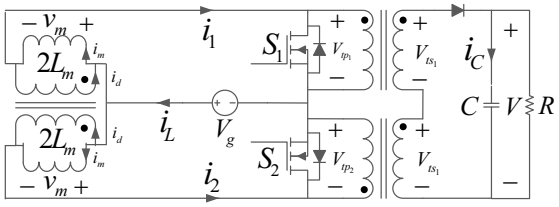
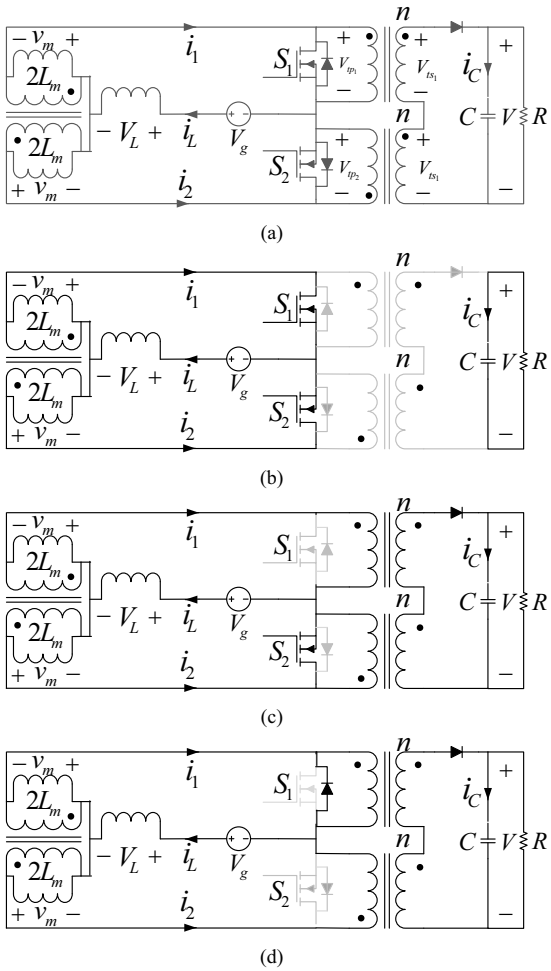


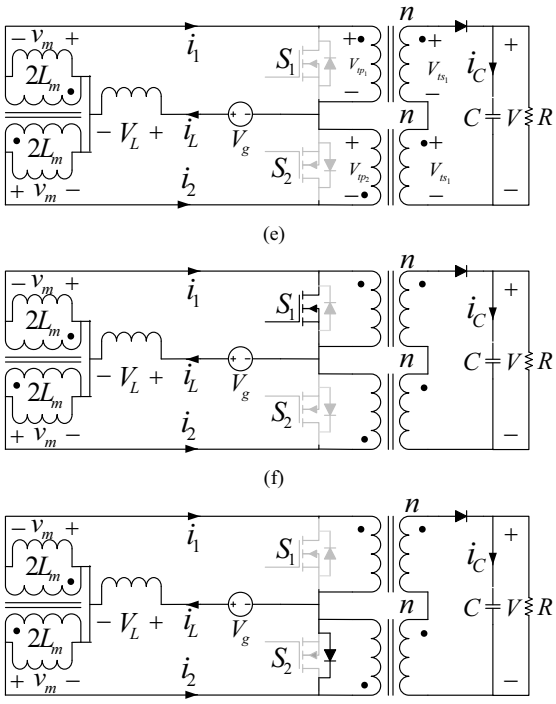
Fig. 5. Simplified PPIBC with two direct coupled inductors

B. Current balancing transformer (CBT):

A single inductor can be connected to two inverse coupled inductors acting as a CBT as shown in Fig. 6a. Figs. 6b-g show the possible operation modes. Fig. 7 shows the corresponding simulation results where switch S_2 has both a turn-off and turn-on delay.



(a) (b) (c) (d)



(e) (f) (g)

Fig. 6. (a) Simplified PPIBC with a CBT (b) charging period (c) turn off delay in S_2 (d) recovery period (e) discharging period (f) turn on delay in S_2 (g) second recovery period (body diode forced to be on)

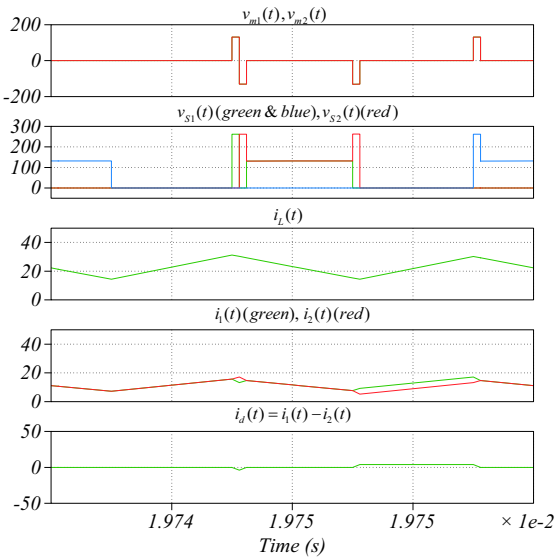


Fig. 7. Simulated waveforms of the converter with CBT

As can be observed from the branch currents after the charging period when the turn off delay occurs, i_2 (red) continues to rise where i_1 starts discharging. Following the turn-off delay period, recovery period starts where body diode of the non-delayed switch S_1 conducts the current difference between i_1 and i_2 until both currents are the same. After that the discharging period starts. Governing equations of the output voltage for this case can be obtained as follows:

$$D(V_g) + D'(V_g - V/(2n)) = 0 \quad (7)$$

$$V = \frac{2n}{D'} V_g \tag{8}$$

The average value of the inductor current can be derived using output capacitor charge balance as:

$$D(-V/R) + (D' - 2d_{off})(i_L(t)/(2n) - V/R) + (d_{off})[(< i_1(t) >_{d_{off}-S} + < i_2(t) >_{d_{off}-D})/n - 2V/R] = 0 \tag{9}$$

which can be reduced to:

$$V/R = D' I_L/(2n) + (d_{off})(< i_m(t) >_{d_{off}-S} - < i_m(t) >_{d_{off}-D})/n \tag{10}$$

In Eq. (10) $d_{off\text{-}S}$ represents the turn off delay of the switch and $d_{off\text{-}D}$ represents the recovery period. Also i_m represents the magnetizing current of the CBT which is effectively the difference current between the two branches. Turn-off delay and the corresponding recovery time are the same because the same amount of voltage drop occurs across the magnetizing inductance of the CBT during both periods. This results in the inductor current as:

$$V/R = D' I_L/(2n) \tag{11}$$

Using Eqs. (8)-(11), average branch current expressions can be derived as:

$$I_1 = I_L/2 + K \qquad I_2 = I_L/2 - K \tag{12}$$

where,

$$K = < i_m(t) >_T = (D) < i_m(t) >_D + d_{off} < i_m(t) >_{d_{off}-S} + d_{off} < i_m(t) >_{d_{off}-D} + (D' - 2d_{off}) < i_m(t) >_{D'-2d_{off}} \tag{13}$$

Since,

$$< i_m(t) >_{d_{off}-S} = < i_m(t) >_{d_{off}-D} = -d_{off} V/(8n f_{SW} L_m) = -d_{off} V_g/(4D' f_{SW} L_m) \tag{14}$$

and,

$$< i_m(t) >_D = < i_m(t) >_{D'-2d_{off}} = 0 \tag{15}$$

The current difference can be written as in Eq. (16),

$$K = -d_{off}^2 V_g/(2D' f_{SW} L_m) \tag{16}$$

Effect of the turn-on delay is different from that of the turn-off delay. It can be observed from Fig. 7 that at the end of the discharging period a difference between i_1 and i_2 occurs due to the turn-on delay of S_2. This results in a longer time where the two branch currents have an offset. Turn-on delay changes the steady state operating point of the converter as in Eq. (17) and Eq. (18).

$$V = \frac{2n}{D' + d_{on}} V_g \tag{17}$$

$$V/R = (D' + d_{on}) I_L/(2n) \tag{18}$$

Similar to the turn-off case the difference current expression can be obtained as in Eq. (19).

$$K = D\, d_{on} V_g/(2 f_{SW} L_m (D' + d_{on})) \tag{19}$$

C. Two separate inductors (TSI)

Instead of the CBT method, each branch can have its own energy storage inductor separately as in Fig. 8. These inductors also act as impedances between the two full bridges limiting the rate of change of the difference current.

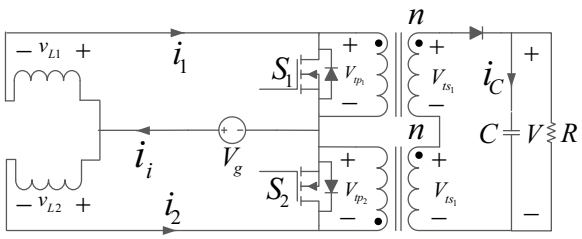


Fig. 8. Simplified PPIBC with a CBT

Normal and extra operation modes of the TSI configuration are the same as Fig. 6b-g. Similar to CBT case turn-off and turn-on delays have different current balancing effects where turn-on delay in switch S_2 produces an offset during the following charging period. Fig. 9 shows the related simulation results where maximum switch stress values appear to be the same as CBT which is two times the nominal voltage reflected through the transformer.

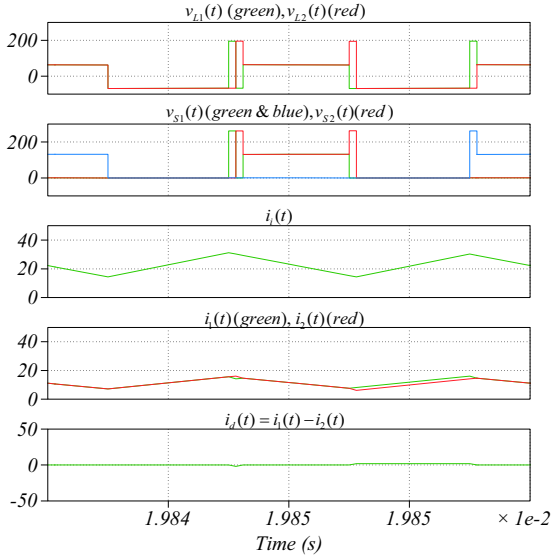


Fig. 9 Simulated waveforms of the converter with TSI

The average current difference between the two branches in TSI case can be derived as in CBT case. Based on Eq. (12) K can be obtain for turn-off and turn-on delays respectively as,

$$K = -d_{off}^2 V_g/(2D' f_{SW} L) \tag{20}$$

$$K = D\, d_{on} V_g/(2 f_{SW} L (D' + d_{on})) \tag{21}$$

D. *Partially coupled inductors (PCI)*

Similar to the previous two methods PCI provides impedance between the two full bridges to limit the rate of change of the difference current (i_d). PCI is composed of two direct coupled inductors with a low coupling factor. Fig. 10 shows simplified PPIBC with PCI acting as a current balancing mechanism. $2L_m$ represents the mutual inductance and 2Lm-2L represents the self (leakage) inductance of the coupled inductor. Possible switching configurations are the same as Fig. 6b-g. Fig. 11 shows the simulated waveforms which are similar to the previous two cases. Voltage drops over the mutual inductances can be observed to be different during the extra operation modes.

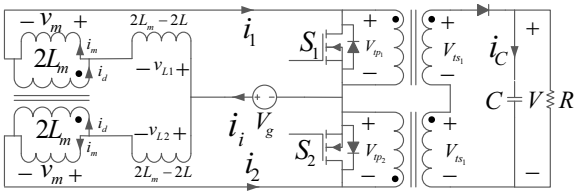


Fig. 10 Simulated waveforms of the converter with TSI

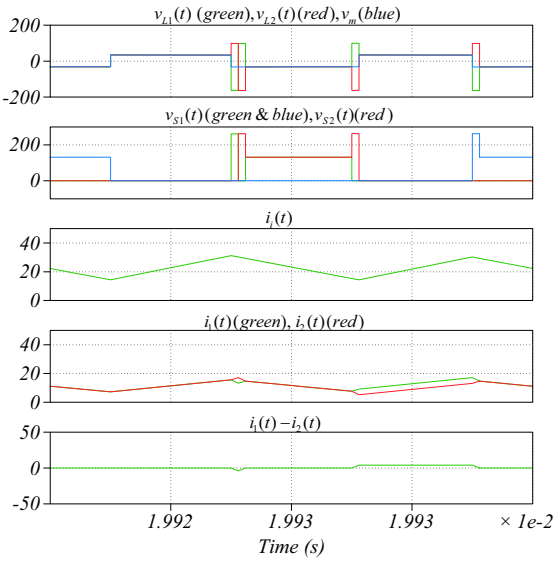


Fig. 11 Simulated waveforms of the converter with PCI

Similar to CBT and TSI case, average difference currents can be obtained analytically for the PCI case. Considering the switching positions in Figs. 6b-g applied to the simplified circuit in Fig. 10, following equations can be derived for a turn-off delayed switch S_2 operation:

$$(D)(L_m/L)(V_g) + (D')(L_m/L)(V_g - V/(2n)) = 0 \quad (22)$$

$$V = \frac{2n}{D'} V_g \quad (23)$$

The output current expression can be obtained as:

$$D(-V/R) + (D' - 2d_{off})(i_L(t)/(2n) - V/R) + (d_{off})[(< i_1(t) >_{d_{off-S}} + < i_2(t) >_{d_{off-D}})/n - 2V/R] = 0 \quad (24)$$

$$V/R = D' I_L/(2n) + (d_{off})(< i_d(t) >_{d_{off-S}} - < i_d(t) >_{d_{off-D}})/n \quad (25)$$

$$V/R = D' I_L/(2n) \quad (26)$$

From here it can be seen that turn-off delay in a switch does not affect the steady state operating point of the converter in PCI case similar to CBT and TSI cases. The average value of the difference current i_d can be calculated as the addition of average i_d values over charging, turn-off delay, recovery (body diode conduction) and discharging periods.

$$K = < i_d(t) >_T = (D) < i_d(t) >_D + d_{off} < i_d(t) >_{d_{off-S}} + d_{off} < i_d(t) >_{d_{off-D}} + (D' - 2d_{off}) < i_d(t) >_{D'-2d_{off}} \quad (27)$$

Since,

$$< i_d(t) >_D = < i_d(t) >_{D'-2d_{off}} = 0 \quad (28)$$

and the remaining periods can be calculated as:

$$< i_d(t) >_{d_{off-S}} = < i_{L1}(t) >_{d_{off-S}} - < i_m(t) >_{d_{off-S}} = \frac{d_{off}}{2f_{sw}}\left(\frac{1}{2L-2L_m}\right)\left(\frac{L-L_m}{L}V_g - \frac{2L-L_m}{2L}\frac{V}{n}\right) - \frac{d_{off}}{2f_{sw}}\left(\frac{1}{2L_m}\right)\left(\frac{L_m}{L}V_g - \frac{L_m}{2L}\frac{V}{n}\right) = -\frac{d_{off}}{8f_{sw}(L-L_m)}\frac{V}{n} = -d_{off}V_g/(4D' f_{SW}(L-L_m)) \quad (29)$$

As mentioned before turn-off delay ($d_{off\text{-}S}$) and recovery period ($d_{off\text{-}D}$) are equal. Based on Eqs. (12,28) and Eq. (29),

$$K = -d_{off}^2 V_g/(2D' f_{SW}(L-L_m)) \quad (30)$$

Again similar to CBT and TSI cases, turn-on delay affects the voltage and current conversion ratios given as in Eqs. (17,18). Turn-on delay average current expression is,

$$K = < i_d(t) >_T = d_{on} < i_d(t) >_{d_{on-S}} + (D - d_{on}) < i_d(t) >_{D-d_{on}} + d_{on} < i_d(t) >_{d_{on-D}} + (D' - d_{on}) < i_d(t) >_{D'-d_{on}} \quad (31)$$

Each component in Eq. (31) can be derived as:

$$< i_d(t) >_{d_{on-S}} = < i_{L1}(t) >_{d_{off-S}} - < i_m(t) >_{d_{off-S}} = \frac{d_{on}}{2f_{sw}}\left(\frac{1}{2L-2L_m}\right)\left(\frac{L-L_m}{L}V_g + \frac{L_m}{2L}\frac{V}{n}\right) - \frac{d_{on}}{2f_{sw}}\left(\frac{1}{2L_m}\right)\left(\frac{L_m}{L}V_g - \frac{L_m}{2L}\frac{V}{n}\right) = \left(\frac{d_{on}}{8f_{sw}(L-L_m)}\frac{V}{n}\right) = d_{on}V_g/(4f_{SW}(D' + d_{on})(L-L_m)) \quad (32)$$

and,

$$< i_d(t) >_{D-d_{on}} = 2 < i_d(t) >_{d_{on-S}} \quad (33)$$

$$< i_d(t) >_{d_{on-D}} = < i_d(t) >_{d_{on-S}} \quad (34)$$

$$< i_d(t) >_{D'-d_{on}} = 0 \quad (35)$$

Using Eqs. (32-35), average difference current for the turn-on delay can be found as,

$$K = D\, d_{on} V_g/(2 f_{SW}(D' + d_{on})(L-L_m)) \quad (36)$$

IV. Experimental Results

Figs. 12-14 show results from different configurations of current balancing for PPIBC. Switching delays in the tested converter occur due to tolerances of the used components. So, compared to the results in the previous sections, experimental waveforms are the results of not only turn-on and turn-off delays in multiple switches but also component value tolerances like inductances. In Fig. 12, single inductor case waveforms can be seen where turn-off delays cause current spikes and turn-on delays cause offsets between the branch currents.

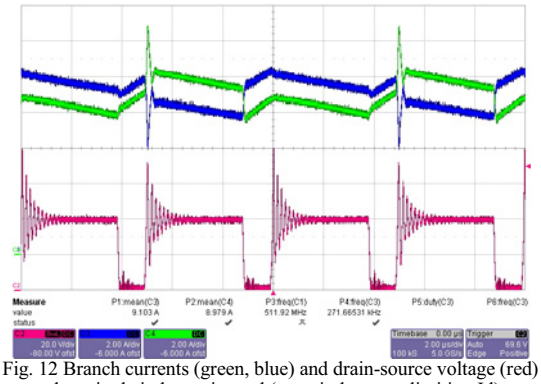


Fig. 12 Branch currents (green, blue) and drain-source voltage (red) when single inductor is used (stray inductance limiting Id)

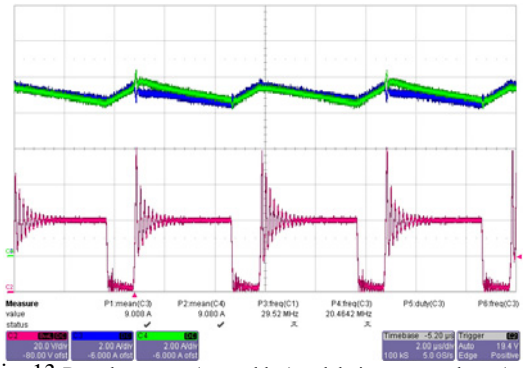


Fig. 13 Branch currents (green, blue) and drain-source voltage (red) when two separate inductors are used

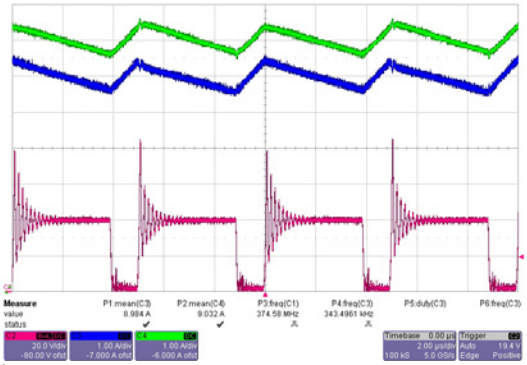


Fig. 14 Branch currents (green, blue) and drain-source voltage (red) when current balancing transformer is used

Fig 13 shows the waveforms for TSI configuration. It can be observed that the tolerance of the two inductors cause slightly different slopes for the two inductor currents. Fig 14 gives the CBT waveforms where branch current waveforms have been given an offset in the scope. Compared to Fig. 12, TSI and CBT configurations seem to suppress the effects of extra operation modes due to switch delays.

V. CONCLUSIONS

In this paper analytical expressions have been derived for single inductor, current balancing transformer (CBT), two separate inductors (TSI) and partially coupled inductors (PCI) for primary parallel isolated boost converter (PPIBC). It has been shown that compared to single inductor; other configurations achieve suppression of current spikes, occurring due to low impedance between the two full bridges in the former case. However an average difference still exists between the branch currents whose value depends on the turn-on/turn-off delay times, switching frequency, input voltage, and the inductance value between the full bridges. There are advantages and disadvantages of each configuration. For example PCI configuration can be implemented as a single component using two E-type powder core halves and winding the two windings around the two side legs. However manufacturing of this component will be expensive since of-the-shelf coil formers are generally designed for center leg windings. TSI configuration achieves current balancing and energy storage at the same time but it has a disadvantage of inductance value tolerance which may easily result in current imbalance. CBT configuration works well for current balancing but it requires two separate components.

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Appendix A3

[A3] M. C. Mira A., J. C. Hernández B., **G. Sen**, O. C. Thomsen, M. A. E. Andersen, "Modeling and control of primary parallel isolated boost converter," IECON 2012 (**Accepted**).

Modeling and Control of Primary Parallel Isolated Boost Converter

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***Abstract*—In this paper state space modeling and closed loop controlled operation have been presented for primary parallel isolated boost converter (PPIBC) topology as a battery charging unit. Parasitic resistances have been included to have an accurate dynamic model. The accuracy of the model has been tested by comparing the calculated and measured loop gains. The designed controller has been implemented in a DSP based control circuit and stable operation of the converter has been achieved.**

***Index Terms*—Battery, fuel cell, isolated boost converter, state-space averaging.**

NOMENCLATURE

$R_{D_{Bat}}$	Battery dynamic resistance
$V_{OC_{Bat}}$	Battery open circuit voltage
r_L	Inductor parasitic resistance
r_{MP}	Primary MOSFET's on resistance
r_p	Transformer primary resistance
r_S	Transformer secondary resistance
r_{MS}	Secondary MOSFET's on resistance
r_{esr}	Capacitor series resistance
v_O'	Reflected output voltage

I. INTRODUCTION

VOLTAGES and/or currents in power electronics circuits need to be regulated around a desired reference value. This is done by adjusting the duty cycle of the controllable switches in a proper way to have the required dynamic behavior. The duty cycle is adjusted by filtering and scaling the error through a compensator which is designed based on an accurate model of the converter [1]. Modeling of switch mode converters have been studied widely in the literature [2]-[5]. A common method used in dc-dc converter modeling is state space averaging [6]-[8]. By using this method, it is possible to represent converter switching states in terms of state space matrices and obtain the small signal model of the converter.

PPIBC is an isolated boost type dc-dc converter topology suitable for low voltage and high current on the input side as shown in Fig. 1 [10]. The two parallel full bridges with their respective transformers work synchronously with the switches in the same positions turning on and off at the same time. This makes the converter operation similar to simple isolated boost converter. The current balancing transformer (CBT) is practically an inverse coupled inductor which only acts as high impedance in case of an imbalance between the two full bridge currents. Fig. 2 shows some key waveforms of operation.

In this paper non-ideal modeling and closed loop control of PPIBC have been investigated. The target application of the converter is a battery charging unit in a fuel cell based vehicle. In fuel cell applications input current is the main parameter to be controlled due to the unique I-V characteristics of the device [9]. For this reason boost type converter topologies are suitable for fuel cell applications, since one of the state variables of the converter is the input inductor current which is in the fuel cell side. On the other hand, battery as a load is quite different in ac small signal terms, compared to pure resistive load which generally is taken as the case for converter dynamic modeling. In addition, due to the battery terminal voltage difference during charging and discharging, the dc operating point of the converter will change modifying the gain of the plant transfer function. That is why designing a controller based on a resistive load may not work for a converter with battery loading in the end application. Based on the above arguments a detailed model has been derived in this paper including component non-idealities. Due to the low dynamics of the fuel cell battery charging system there is no high bandwidth requirement for the converter. In addition, as a result of the phase erosion in the control loop due to signal conditioning and digital control delay, an upper limit naturally appears in the achievable control loop bandwidth. Therefore, a DSP based controller has been implemented whose pole and zero locations have been selected to achieve a 1 kHz loop bandwidth. The compensated loop gain and phase of the converter have been measured and compared to the derived model.

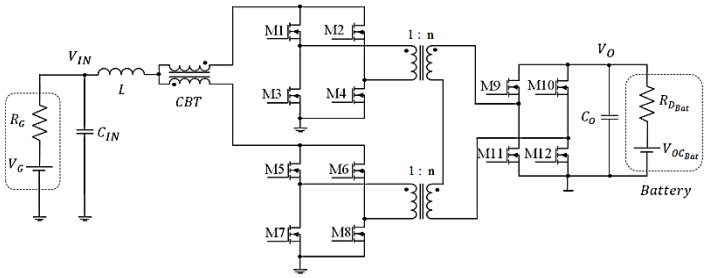

Fig. 1. Primary parallel isolated boost converter with synchronous rectification.

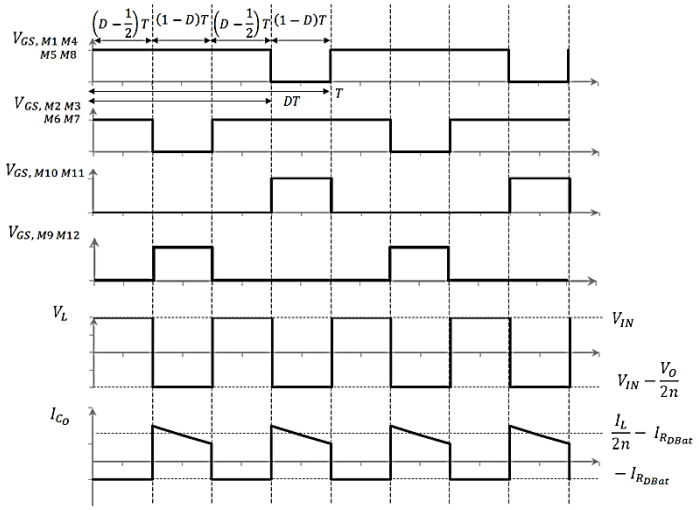

Fig. 2. Steady state operating waveforms.

II. CONVERTER MODELING

In this section PPIBC will be modeled including parasitic resistances of the circuit components. The output voltage is fixed by the battery, thus to achieve fuel cell power regulation only inductor current will be controlled. In order to obtain the duty ratio-to-inductor current transfer function state space averaging is performed by obtaining the two linear sub-circuits in the charging and discharging switching states. Each switching state can be expressed in terms of state space equations, Eq. (1) and Eq. (2). However, the output equation (2) will not be employed since inductor current is already a state variable.

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t) \tag{1}$$

$$y(t) = Cx(t) + Du(t) \tag{2}$$

Fig. 3 shows the inductor charging period where all the primary switches are conducting, the secondary switches are off and the load current is supplied by the output capacitor. A simplified version of Fig. 3 can be obtained by reflecting the secondary side components to the primary side as shown in Fig. 4.

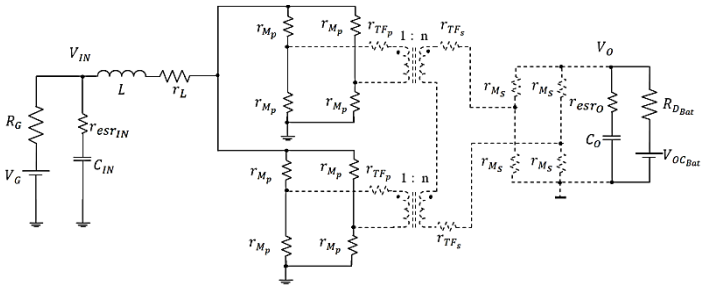

Fig. 3. Charging period equivalent circuit.

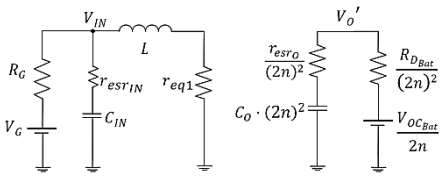

Fig. 4. Simplified charging period sub-circuit.

Parasitic resistances of the input inductor and the primary switches can be grouped as equivalent resistance $r_{eq1} = r_L + r_{M_P}/2$; also the reflected output voltage is defined as $v_o' = v_o/2n$. The dynamic equations during the charging state can be obtained by evaluating the derivatives of the inductor current and the input and output capacitor voltages as shown in (3), (4) and (5).

$$L \cdot \frac{di_L(t)}{dt} = v_{IN}(t) - i_L(t) \cdot r_{eq1} \tag{3}$$

$$C_{IN} \cdot \frac{dv_{C_{IN}}(t)}{dt} = \frac{v_{IN}(t) - v_{C_{IN}}(t)}{r_{esr_{IN}}} \tag{4}$$

$$C_O \cdot (2n)^2 \cdot \frac{dv_{C_O}(t)}{dt} = \frac{v_O'(t) - v_{C_O}(t)}{r_{esr_O}/(2n)^2} \tag{5}$$

Expressions of v_{IN} and v_O' for the charging period are given in (6) and (7).

$$v_{IN}(t) = \frac{V_G \cdot r_{esr_{IN}} + v_{C_{IN}}(t) \cdot R_G - i_L(t) \cdot \left(R_G \cdot r_{esr_{IN}}\right)}{R_G + r_{esr_{IN}}} \tag{6}$$

$$v_O'(t) = \frac{\frac{V_{OC_{Bat}}}{2n} \cdot r_{esr_O} + v_{C_O}(t) \cdot R_{D_{Bat}}}{R_{D_{Bat}} + r_{esr_O}} \tag{7}$$

Rearranging (3), (4) and (5) in the state space matrix form given in Eq. (8) results in Eq. (9).

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \tag{8}$$

Fig. 5 shows the inductor discharge period where two diagonal switches are conducting in each full bridge on the primary side. The two transformers are actively transferring power through two corresponding diagonal switches on the secondary side.

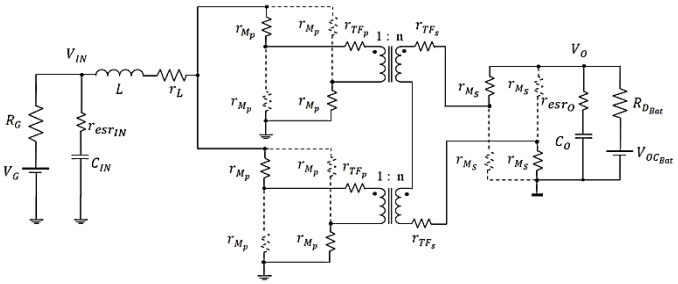

Fig. 5. Discharging period equivalent circuit.

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_{IN}}(t) \\ v_{C_O}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(r_{eq1} + \frac{r_{esr_{IN}} \cdot R_G}{R_G + r_{esr_{IN}}}\right) & \frac{R_G}{L\left(R_G + r_{esr_{IN}}\right)} & 0 \\ -\frac{R_G}{C_{IN}\left(R_G + r_{esr_{IN}}\right)} & -\frac{1}{C_{IN}\left(R_G + r_{esr_{IN}}\right)} & 0 \\ 0 & 0 & -\frac{1}{C_O\left(R_{D_{Bat}} + r_{esr_O}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_{IN}}(t) \\ v_{C_O}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esr_{IN}}}{L\left(R_G + r_{esr_{IN}}\right)} & 0 \\ 0 & 0 \\ \frac{1}{C_{IN}\left(R_G + r_{esr_{IN}}\right)} & 0 \\ 0 & \frac{1}{2C_O n\left(R_{D_{Bat}} + r_{esr_O}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_G \\ V_{OC_{Bat}} \end{bmatrix} \tag{9}$$

Simplifying the sub-circuit in Fig. 5 leads to the circuit shown in Fig. 6. Here the two transformers are combined to a single transformer with an equivalent turn ratio. Furthermore, the transformer in Fig. 6 can also be eliminated by reflecting the impedances on the secondary side to the primary side as shown in Fig. 7.

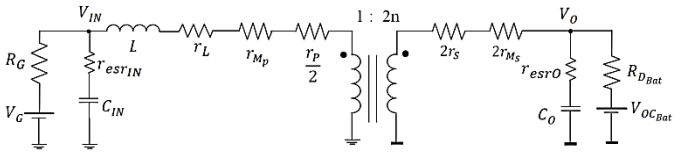

Fig. 6. Equivalent discharging period sub-circuit.

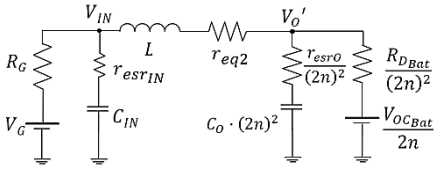

Fig. 7. Simplified sub-circuit with reflected secondary side impedances.

The equivalent resistance r_{eq2} is given by Eq. (10).

$$r_{eq2} = r_L + r_{M_P} + \frac{r_P}{2} + \frac{2r_S}{(2n)^2} + \frac{2r_{M_S}}{(2n)^2} \tag{10}$$

The inductor and capacitor equations for the discharging switching state can be written as in Eq. (11), Eq. (12) and Eq. (13).

$$L \cdot \frac{di_L(t)}{dt} = V_{IN}(t) - i_L(t) \cdot r_{eq2} - v_O'(t) \tag{11}$$

$$C_{IN} \cdot \frac{dv_{C_{IN}}(t)}{dt} = \frac{V_{IN}(t) - v_{C_{IN}}(t)}{r_{esr_{IN}}} \tag{12}$$

$$C_O \cdot (2n)^2 \cdot \frac{dv_{C_O}(t)}{dt} = \frac{v_O'(t) - v_{C_O}(t)}{r_{esr_O}/(2n)^2} \tag{13}$$

Expressions of v_{IN} and $v_O{}'$ for the discharging state are given in (14) and (15).

$$v_{IN}(t) = \frac{V_G \cdot r_{esr_{IN}} + v_{C_{IN}}(t) \cdot R_G - i_L(t) \cdot \left(R_G \cdot r_{esr_{IN}}\right)}{R_G + r_{esr_{IN}}} \tag{14}$$

$$v_O'(t) = \frac{V_{OC_{Bat}}/2n \cdot r_{esr_O} + v_{C_O}(t) \cdot R_{D_{Bat}} + \frac{i_L(t)}{(2n)^2} \cdot \left(R_{D_{Bat}} \cdot r_{esr_O}\right)}{R_{D_{Bat}} + r_{esr_O}} \tag{15}$$

Eq. (11), Eq. (12) and Eq. (13) can be written in the form of Eq. (16). The state and input matrices of the discharging subinterval can be expressed as in Eq. (17).

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \tag{16}$$

The two switching states are averaged over the switching period using Eq. (18) and Eq. (19).

$$A = A_1 \cdot d + A_2 \cdot (1 - d) \tag{18}$$

$$B = B_1 \cdot d + B_2 \cdot (1 - d) \tag{19}$$

All the variables are perturbed around a quiescent operating point X. This results in $(X + \hat{x})$ where $X \gg \hat{x}$. Eliminating the dc and the second order terms gives the first order linear model shown in Eq. (20).

$$\dot{\hat{x}} = A \cdot \hat{x} + B \cdot \hat{v}_G + [(A_1 - A_2)X + (B_1 - B_2)V_G] \cdot \hat{d} \tag{20}$$

The steady state solution in Eq. (20) can be obtained by manipulation of matrices A and B as shown in Eq. (21).

$$X = -A^{-1} \cdot B \cdot V_g \tag{21}$$

The duty cycle-to-inductor current transfer function is obtained by setting the input voltage perturbation to zero.

$$G_{i_L} = \left.\frac{\hat{\imath}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_G(s)=0} \tag{22}$$

The symbolic expression for G_{i_L} has been obtained using MATLAB; however, it has not been included in here due to space limitation. The gain and phase plots of Eq. (22), required for controller design purposes, has been obtained using the values given in Table I and Table II, as shown in Fig.9 and Fig. 10.

TABLE I
PARAMETERS OF THE CONVERTER

Input Voltage	$36V$
Output Voltage	$48V$
Turn ratio	$1:3$
Inductor	$13.4\ \mu H$
Transformer and inductor core material	Ferrite 3F3
Capacitor C_{IN}	$40\ \mu H$
Capacitor C_O	$120\ \mu H$
Switches M1-M8	IPA075N15N3 G
Switches M9-M12	FDH055N15A
Switching frequency	$50\ kHz$

TABLE II
CONVERTER PARASITIC RESISTANCES

r_L	$3.9\ m\Omega$
r_{MP}	$7.5\ m\Omega$
r_p	$3.5\ m\Omega$
r_S	$0.4\ m\Omega$
r_{MS}	$5.9\ m\Omega$
$r_{esr_{IN}}$	$3.15\ m\Omega$
r_{esr_O}	$1.1\ m\Omega$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_{IN}}(t) \\ v_{C_O}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(r_{eq2} + \frac{r_{esrO} \cdot R_{D_{Bat}}}{4n^2\left(R_{D_{Bat}} + r_{esrO}\right)} + \frac{r_{esr_{IN}} \cdot R_G}{R_G + r_{esr_{IN}}}\right) & \frac{R_G}{L\left(R_G + r_{esr_{IN}}\right)} & -\frac{R_{D_{Bat}}}{L\left(R_{D_{Bat}} + r_{esrO}\right)} \\ -\frac{R_G}{C_{IN} \cdot \left(R_G + r_{esr_{IN}}\right)} & -\frac{1}{C_{IN}\left(R_G + r_{esr_{IN}}\right)} & 0 \\ \frac{R_{D_{Bat}}}{4C_O n^2\left(R_{D_{Bat}} + r_{esrO}\right)} & 0 & -\frac{1}{C_O\left(R_{D_{Bat}} + r_{esrO}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_{IN}}(t) \\ v_{C_O}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esr_{IN}}}{L\left(R_G + r_{esr_{IN}}\right)} & -\frac{r_{esr_{IN}}}{2nL\left(R_{D_{Bat}} + r_{esrO}\right)} \\ \frac{1}{C_{IN}\left(R_G + r_{esr_{IN}}\right)} & 0 \\ 0 & \frac{1}{2nC_O\left(R_{D_{Bat}} + r_{esrO}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_G \\ V_{OC_{Bat}} \end{bmatrix} \tag{17}$$

The dynamic resistance of a battery varies significantly depending on the battery state of charge (SOC) and state of health (SOH) [11]. Moreover, the battery terminal voltage will be dependent on these parameters as well as on the charging and discharging current levels. The dynamic resistance together with the instantaneous terminal voltage affect the dc gain of the duty cycle-to-inductor current transfer function and the converter steady state operating point. Therefore, in battery loaded applications, a detailed modeling of the battery has to be performed taking into consideration the variations of the dynamic behavior depending on both aging and SOC. In the end application this will affect the control loop behavior both in short and long term reducing the reliability of the system. Dynamic characterization of lead-acid battery is out of scope of this paper and will be the subject of another work. However, in order to be able to test the accuracy of the derived converter model, several measurements of the battery dynamic resistance and the battery terminal voltage are performed at the converter operating conditions. The batteries used in this experiment are Haze HZB-EV12-26 which are rated for 12 volts and 26 Ah. The impedance measurement results are shown in Fig. 8.

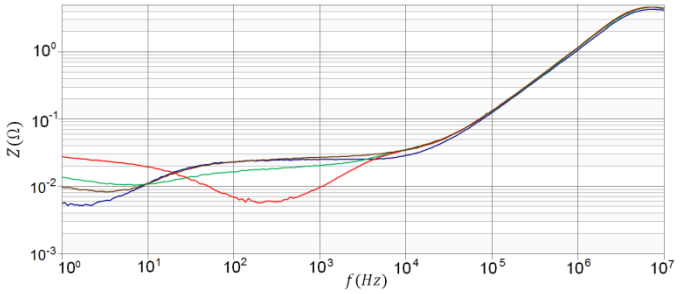

Fig. 8. Battery bank individual impedance measurements.

The battery dynamic resistance value has been taken as the series combination of the four individual battery impedances @ 1 kHz which is the desired loop crossover frequency. According to the measurements of Fig. 8 the equivalent resistance value is $R_{D_{Bat}} \approx 80\ m\Omega$.

Fig. 9 shows the simulated gain and phase plots of the duty cycle-to-inductor current transfer function for two cases. Blue line shows the converter operated with battery as a load and the green line presents a pure resistive loading for the same converter power level. It can be observed that due to the low dynamic resistance of the battery the transfer function of the converter behaves similar to a first order system. The complex poles appearing at the converter natural resonant frequency in the pure resistive loading case are separated in the case of battery loading.

Fig. 10 shows the simulated effect of introducing parasitic elements in the converter model. The gain reduction at low frequencies is due to the fact that the parasitic resistances are in the same value range with the battery bank impedance. Ignoring the parasitic elements during the modeling process will result in a deviation of the open loop transfer function crossover frequency location.

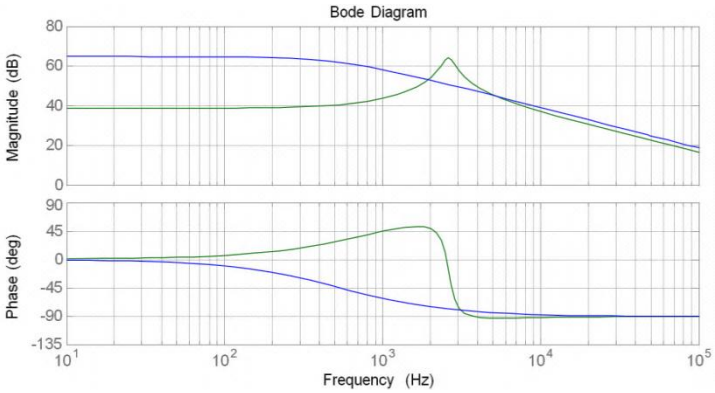

Fig. 9. Calculated converter transfer function with resistive load (green trace) and with a battery as a load (blue trace) for the same power level.

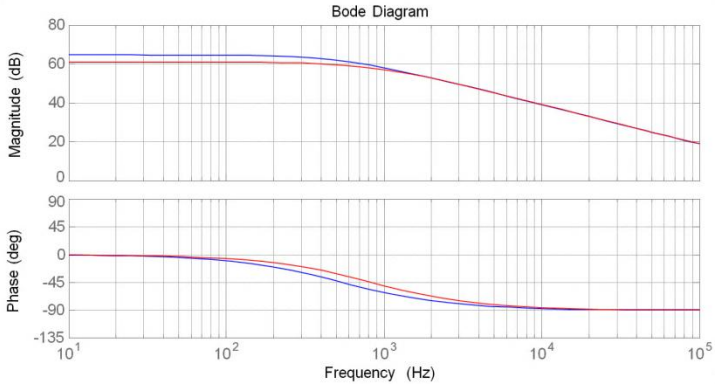

Fig. 10. Calculated control to inductor current transfer function with (red trace) and without (blue trace) parasitic resistances.

III. Implemented Prototype

A prototype of PPIBC has been constructed using planar magnetic elements as shown in Fig. 11. The control law has been implemented using TMS320F28035 which is a 32 bit microcontroller. The MOSFETs are driven by IR2110's connected to the microcontroller through ISO7241 capacitive isolators. The inductor current is measured by a LEM Hall effect current transducer, LAS 100-TP, with $\pm 100A$ measurement range. The transducer signal is conditioned by an operational amplifier as shown in Fig. 15 configured in differential mode. The signal is low pass filtered to avoid aliasing and a dc offset is introduced. The gain is adjusted to cover the ADC voltage range of the microcontroller which is from 0 to 3.3 V. Configuration of the control circuit is given in Fig. 12 as a block diagram. Fig. 13 shows the closed loop control block diagram.

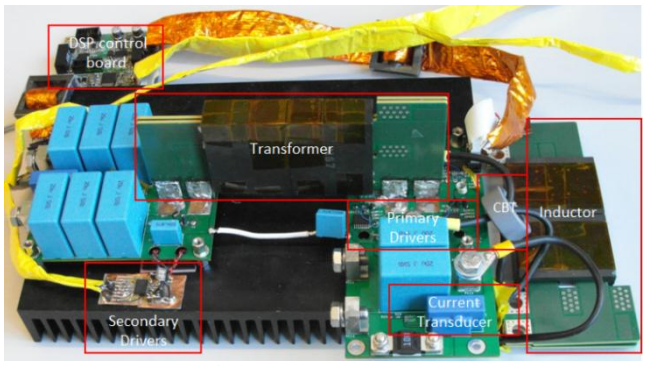

Fig. 11 Converter prototype

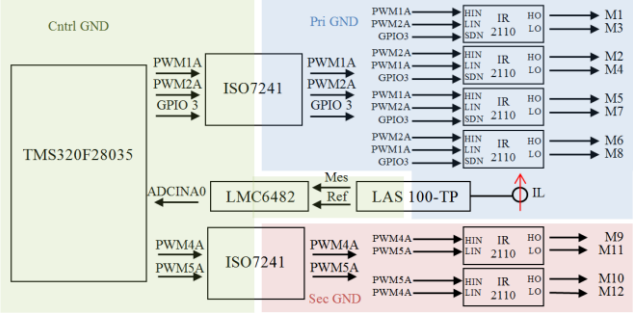

Fig. 12. Control Circuitry Diagram.

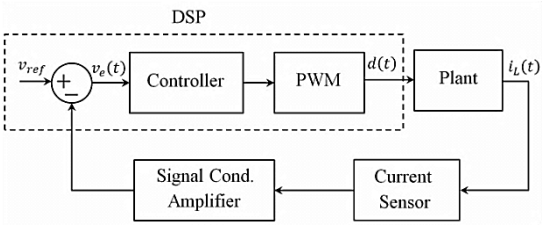

Fig. 13. Closed loop control block diagram.

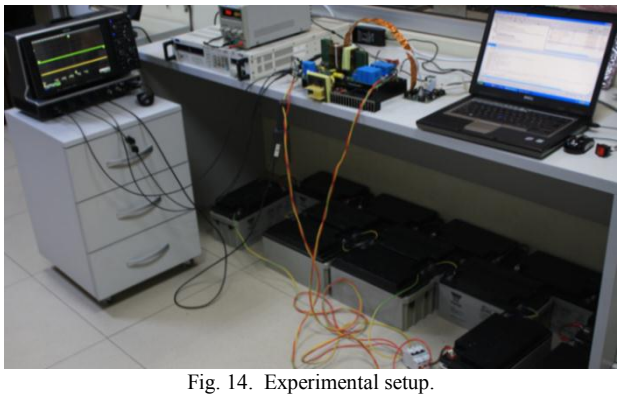

Fig. 14. Experimental setup.

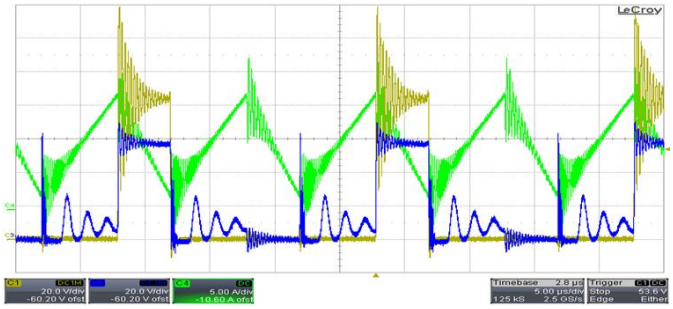

Fig. 15. Converter operating waveforms, primary drain to source voltage (light brown, 20V/div), secondary drain to source voltage (blue, 20V/div) and inductor current (green, 5A/div). Time scale: 5µs/div.

The test setup of the converter is shown in Fig. 14. The steady state operation of the PPIBC is shown in Fig. 15. High frequency resonances can be observed due to the interaction of parasitic capacitances and inductances in the circuit.

In order to see the effect of the signal conditioning amplifier to the gain and phase of the loop, its transfer function has been derived as in Eq. (23) based on Fig. 16. By using the values given in Table III the signal conditioning amplifier transfer function is drawn. A small signal measurement is also performed in order to verify the accuracy of the calculated transfer function. Fig. 17 shows the measured and calculated signal conditional amplifier transfer function.

Fig. 18 shows the measured and the calculated transfer function of the control algorithm built in DSP together with the sampling, calculation and PWM reconstruction delays.

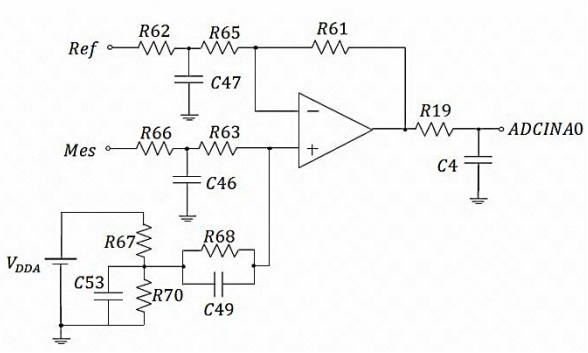

Fig. 16. Signal conditioning amplifier.

TABLE III
PARAMETERS OF THE SIGNAL CONDITIONING AMPLIFIER

$R62, R66$	$1\ k\Omega$
$R65, R63$	$100\ k\Omega$
$R61$	$220\ k\Omega$
$R68$	$330\ k\Omega$
$R67$	$1.2\ k\Omega$
$R70$	$820\ \Omega$
$R19$	$270\ \Omega$
$C46$	$10\ nF$
$C47, C53, C4$	$100\ nF$
$C49$	$100\ pF$

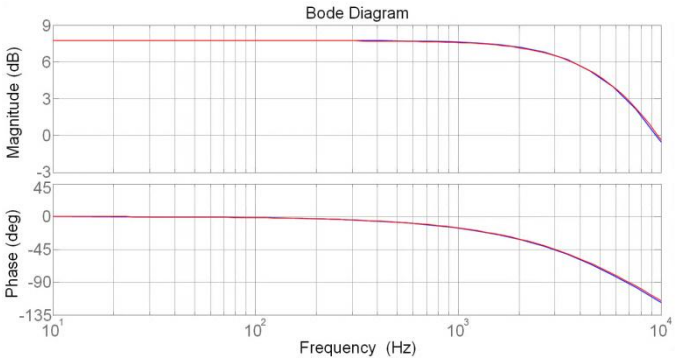

Fig. 17. Signal conditioning amplifier calculated (blue) and measure (red) transfer function.

$$\frac{V_{ADCINA0}}{V_{mes}} = \frac{R61 \cdot Z_{eq1} \cdot \left(\frac{1}{R61} + \frac{1}{Z_{eq2}}\right)}{\left(R63 + Z_{eq1}\right)} \cdot \frac{1}{\left(\frac{R66}{R63 + Z_{eq1}} + C46 \cdot R66 \cdot s + 1\right)(1 + s \cdot R19 \cdot C4)} \qquad (23)$$

$$Z_{eq1} = R68||C49 + R70||R67||C53 \qquad Z_{eq2} = R62||C47 + R65$$

Due to the fact that the duty cycle-to-inductor current transfer function behaves as a first order system, the implemented control law, shown in Fig.18, is formed by an integrator and a zero placed before the loop crossover frequency to obtain the required phase margin.

The compensated loop transfer function is calculated including the signal conditioning amplifier transfer function, the microcontroller delay and the current transducer gain. The input voltage and the output battery terminal voltage for an inductor current of $I_L = 10\,A$ are measured to be $V_G = 33.6\,V$ and $V_o = 56.1\,V$. These values are used in the obtained model assuming that the output resistance of the input voltage source has a negligible value at the frequencies of interest.

The calculated and measured open loop transfer function is shown in Fig. 19. At low frequencies a small deviation in the phase plot is observed which can be the result of the combined effect of non-ideal integrator implemented inside the DSP and the low frequency increase of the battery dynamic resistance. Both gain and phase plots have close matching due to the fact that parasitic and delay effects have been included during the modeling process.

Fig. 20 shows a current reference step change experiment from 27A to 40A. A settling time of 0.5 ms is observed which is compatible with the 1 kHz measured crossover frequency of the loop gain. An important detail regarding the relation between crossover frequency and the battery as a load is the possible variation in the loop gain due to the changing current level. This is due to the current dependence of battery terminal voltage which limits the available bandwidth since further increase in gain will lower the phase margin significantly as can be observed in Fig. 19.

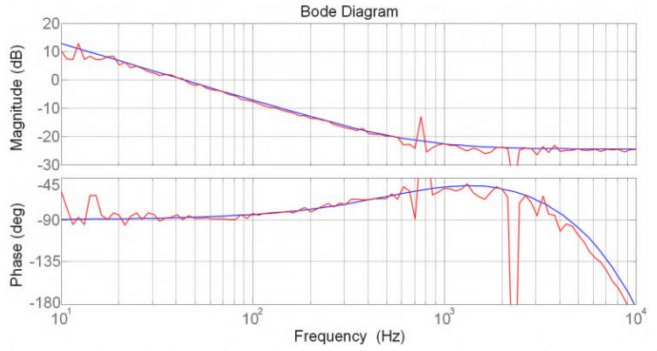

Fig. 18. Gain and phase plots of calculated (blue) and measured (red) control algorithm including the delays.

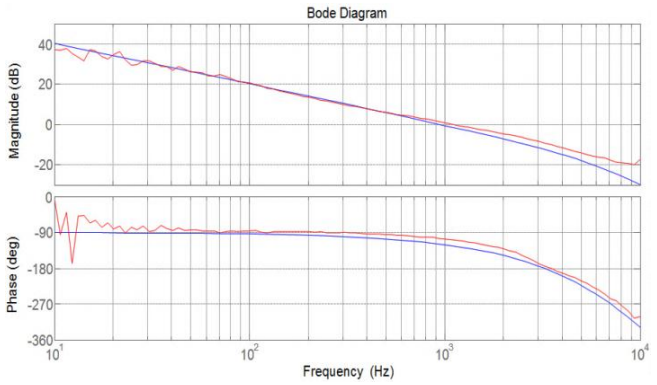

Fig. 19. Calculated (blue trace) and measured (red trace) loop gain.

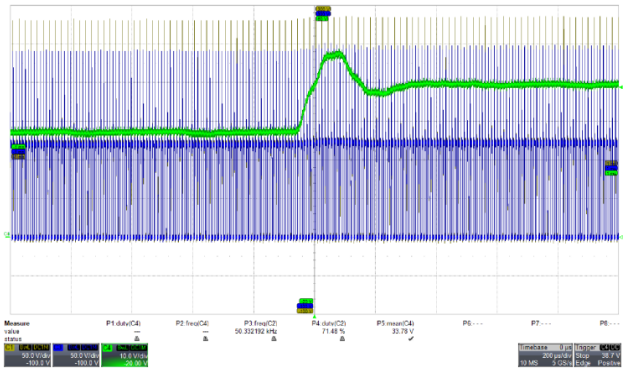
Fig. 20. Current reference step response. Primary drain to source voltage (light brown, 50V/div), secondary drain to source voltage (blue, 50V/div) and inductor current (green, 10A/div). Time scale: 200µs/div.

IV. Conclusion

In this paper primary parallel isolated boost converter (PPIBC) loaded with battery has been investigated from modeling and control aspects. A non-ideal converter circuit has been taken into consideration to derive the state space averaged converter model since the series resistance of the battery and the parasitic element values are in the same value range, which is not the case in a pure resistive load for the same power level. The battery bank impedance has also been measured and the impedance value around the crossover frequency has been used. The time delays of the loop due to the digital implementation have also been considered in the model as well as the transfer function of the signal conditioning circuit. Based on this detailed model a simple controller has been designed and implemented. The measured loop gain and phase have been compared to the calculated model achieving close match.

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Appendix A4

[A4] J. C. Hernández B., M. C. Mira A., **G. Sen**, O. C. Thomsen, M. A. E. Andersen, "Primary parallel isolated boost converter with bidirectional operation," VPPC 2012 (**Accepted**).

Primary Parallel Isolated Boost Converter with Bidirectional Operation

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***Abstract*—This paper presents a bidirectional dc/dc converter operated with batteries both in the input and output. Primary parallel isolated boost converter (PPIBC) with transformer series connection on the high voltage side is preferred due to its ability to handle high currents in the low voltage side. The converter has been modeled using non-ideal components and operated without any additional circuitry for startup using a digital soft-start procedure. Simulated and measured loop gains have been compared for the validity of the model. On-the-fly current direction change has been achieved between input and output battery banks with a defined ramp.**

***Index Terms*—Bidirectional, startup, battery.**

NOMENCLATURE

$R_{D\,Bat}$	Battery dynamic resistance
$V_{OC\,Bat}$	Battery open circuit voltage
r_L	Inductor parasitic resistance
r_{MP}	Primary MOSFET's on resistance
r_p	Transformer primary resistance
r_S	Transformer secondary resistance
r_{MS}	Secondary MOSFET's on resistance
r_{ESR}	Capacitor series resistance

I. INTRODUCTION

SUPERCAPACITOR banks and batteries with bidirectional converters are being used for supporting low dynamic renewable energy sources like fuel cells as shown in Fig. 1. Also they allow regeneration in electric vehicle applications by recovering the kinetic energy during the braking process. Different bidirectional dc-dc converter topologies have been proposed and investigated in the literature so far [1]-[3].

PPIBC is an efficient solution for low voltage high current applications [4]-[5]. The schematic and waveforms of the proposed bidirectional converter are shown in Fig. 2. Due to the transformer series connection on the secondary side, the current on each parallel primary stage is forced to be equal. However, different stray inductances in the current path or mismatches in the gate drive signal can cause the input current of each full bridge deviate from each other. In order to prevent this situation a current balancing transformer (CBT) is inserted to the circuit in series with the input inductor [6]. The CBT, which is implemented as an inverse coupled inductor, shows high impedance in between the two parallel primary stages and keeps the branch currents to be equal.

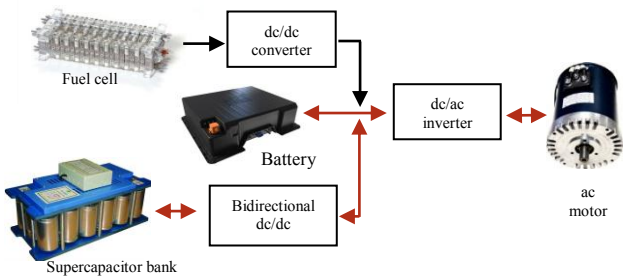

Fig. 1. Supercapacitor and bidirectional converter integration into a fuel cell powered drive train.

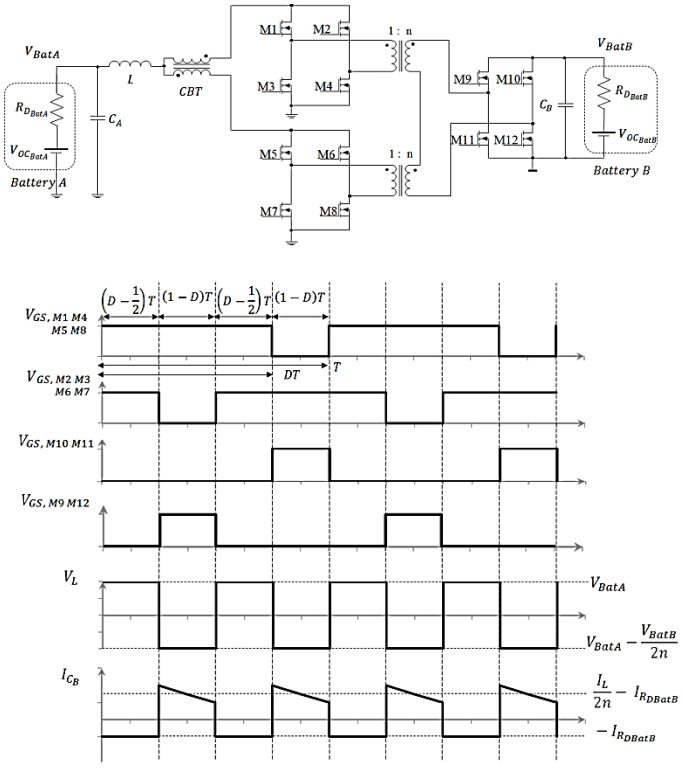

Fig. 2. Converter schematic (up) and boost mode steady state operating waveforms (down).

In this topology, parallel primary power stages share the same control signals with the same phase switching sequence for the corresponding switches, which allows a simpler control, similar to simple isolated boost converter. Output rectification unit as well as input and output filters are common to both of the parallel primary stages. The paralleling method splits the critical high ac-current-loop into

two smaller loops. Each of the smaller loops only needs to switch half of the input current thereby achieving higher conversion efficiency. Since the two transformers share the same input current and have their secondary windings connected in series, a higher turns-ratio transformer can be replaced by two lower turns-ratio transformers, which allows a simple design and manufacturing of the transformers.

In this paper bidirectional operation of the PPIBC is studied. An accurate dynamic model of the converter has been derived taking into consideration the component non-idealities. Simple battery models with internal impedances for both low and high voltage sides are also included in the model. PPIBC has been reduced to a simple boost converter in order to write the state space equations. Gain and phase plots of the compensated loop have been obtained from both the derived model and the experimental setup. Stable operation has been achieved for both directions with a digital startup procedure.

II. Converter Modeling

In general small signal modeling of dc-dc converters assume pure resistive loading, which is not the case most of the time. For example in case of battery loading, small internal impedance of the battery will dominate the load characteristics. If a controller is designed based on pure resistive loading and operated with batteries, unexpected dynamic behavior may be observed. This is not desired in battery charging applications due to the sensitivity of the current to the variations in the control parameter which is the duty cycle. Consequently, it is very important to use a precise model and confirm the stability of the operation by loop measurements [7].

In this research simple battery model has been preferred, which is an ideal voltage source with a voltage value equal to the battery open circuit voltage in series with the battery dynamic resistance. With the input and output voltages fixed by the batteries, the variable to control is the inductor current. All the converter parasitic resistances have been included in the model because they are in the same range with the battery dynamic resistances and consequently will affect the dc gain of the converter.

The dynamic behavior of the converter does not change from one direction to the other since the same differential equations will govern the circuit independent of the power flow direction. That is why a single model is derived for both operating modes.

Fig.3 shows the first state of the converter that corresponds to the charging state in boost mode and the discharging state in buck mode. Fig. 4 shows the simplified version of Fig. 3 where the two transformers are combined into an equivalent transformer with a turn ratio of 1: 2n. All the components are reflected to the inductor side and parasitic resistances are combined into an equivalent resistance (r_{eq1}).

Fig. 5 presents the second state of operation corresponding to the discharging state of the boost mode and the charging state of the buck mode. Similar to the previous state the circuit is reduced to a simpler form as shown in Fig. 6.

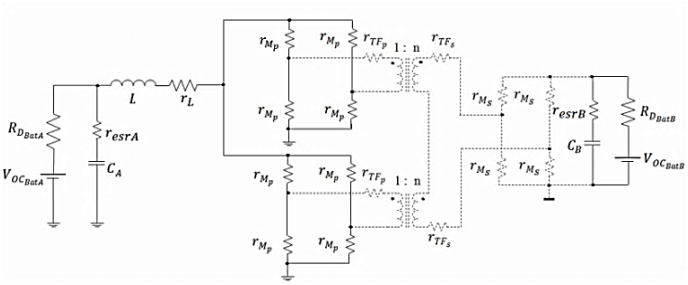

Fig. 3. Converter first state with parasitic resistances.

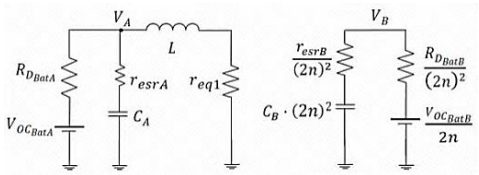

Fig. 4. Simplified equivalent circuit for the converter first state.

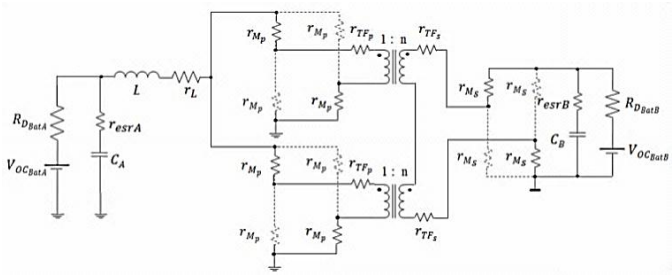

Fig. 5. Converter second state with parasitic resistances.

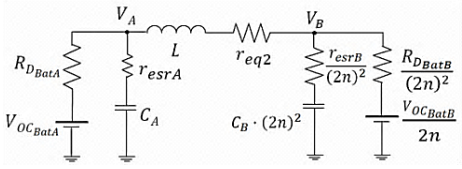

Fig. 6. Simplified equivalent circuit for the converter second state.

The equivalent resistances in Fig. 4 and Fig. 6 are given by (1) and (2).

$$r_{eq1} = r_L + r_{MP}/2 \tag{1}$$

$$r_{eq2} = r_L + r_{MP} + \frac{r_P}{2} + \frac{2r_S}{(2n)^2} + \frac{2r_{M_S}}{(2n)^2} \tag{2}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(r_{eq1} + \frac{r_{esrA}\cdot R_{D_{BatA}}}{R_{D_{BatA}} + r_{esrA}}\right) & \frac{R_{D_{BatA}}}{L\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ -\frac{R_{D_{BatA}}}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & -\frac{1}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ 0 & 0 & -\frac{1}{C_B\left(R_{D_{BatB}} + r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ \frac{1}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ 0 & \frac{1}{2C_B n\left(R_{D_{BatB}} + r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_{OC_{BatA}} \\ V_{OC_{BatB}} \end{bmatrix} \tag{5}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(r_{eq2} + \frac{r_{esrB}\cdot R_{D_{BatB}}}{4n^2\left(R_{D_{BatB}} + r_{esrB}\right)} + \frac{r_{esrA}\cdot R_{D_{BatA}}}{R_{D_{BatA}} + r_{esrA}}\right) & \frac{R_{D_{BatA}}}{L\left(R_{D_{BatA}} + r_{esrA}\right)} & -\frac{R_{D_{BatB}}}{L\left(R_{D_{BatB}} + r_{esrB}\right)} \\ -\frac{R_{D_{BatA}}}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & -\frac{1}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ \frac{R_{D_{BatB}}}{4C_B n^2\left(R_{D_{BatB}} + r_{esrB}\right)} & 0 & -\frac{1}{C_B\left(R_{D_{BatB}} + r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ \frac{1}{C_A\left(R_{D_{BatA}} + r_{esrA}\right)} & 0 \\ 0 & \frac{1}{2C_B n\left(R_{D_{BatB}} + r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_{OC_{BatA}} \\ V_{OC_{BatB}} \end{bmatrix} \tag{6}$$

Based on the simplified circuits for both operating states, state space matrixes can be written in the form of (3) and (4) as in (5) and (6), for the first and the second converter states respectively.

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \quad (3)$$

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \quad (4)$$

The state and input matrixes A and B are obtained by averaging the individual matrixes for each state over a period as shown in (7) and (8).

$$A = A_1 \cdot d + A_2 \cdot (1 - d) \quad (7)$$

$$B = B_1 \cdot d + B_2 \cdot (1 - d) \quad (8)$$

After perturbing the circuit around a steady state operating point, the first order terms are collected to obtain the linear model as in (9).

$$\hat{\dot{x}} = A \cdot \hat{x} + B \cdot \hat{u} + [(A_1 - A_2)X + (B_1 - B_2) \cdot U] \cdot \hat{d} \quad (9)$$

The term X corresponds to the steady state solution given in (10).

$$X = -A^{-1} \cdot B \cdot U \quad (10)$$

Finally the small signal expressions of the state variables can be obtained by making $\hat{u}$ equal to zero and applying the Laplace transform to (9) obtaining (11).

$$\hat{x} = (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U] \cdot \hat{d} \quad (11)$$

It is important to notice why the same plant transfer function is obtained independent of the power flow direction. If we consider the boost operating mode, the inductor charging subinterval is defined as dT which corresponds to discharging subinterval for buck mode defined as $(1-d)T$. This duality is valid for all the converter dynamic expressions between buck and boost operating modes. Consequently, the final state equations remain the same independent of the power flow direction as shown in Table I.

III. Experimental Results

A DSP based digital controlled PPIBC has been built and tested as shown in Fig. 7. The two transformers are integrated into the same magnetic core structure. This integrated magnetic component is constructed with four halves of ELP64/10/50 based on N87 core material. The input inductor is built using four halves of E64/10/50 based on 3F3 material. The windings in both magnetic components are implemented using PCB boards with FR4 material. The inductor current is sensed by a Hall Effect current transducer LAS100-TP. The current measurement is low pass filtered by a differential amplifier to avoid aliasing at the ADC input.

The prototype is connected to two battery banks at the low and high voltage side each. The battery bank on the low voltage side is formed by three series connected lead-acid batteries Haze HZB-EV12-26 which are rated for 12 volts and 26 Ah. On the high voltage side same type batteries have been used; in this case four of them in series. The battery impedance is measured and the obtained value at 1 kHz is used in the derived dynamic model to match the gain at the desired converter crossover frequency. The converter parameters are shown in Table II and the parasitic resistances are presented in Table III. The magnetic component parasitic resistances correspond to the measured values at 1 kHz.

A simulation using LTspice IV is used to validate the derived model by comparing the gain and phase plots. The steady state value of the inductor current is selected to be 10A in both converter directions. The converter duty cycle is calculated from the converter dc steady state solution given in Eq. (10). Fig. 8 and Fig. 9 present the calculated and simulated gain and phase plots of the converter duty cycle-to-inductor current transfer function with a steady inductor duty cycle of 0.5095. for $I_L = 10A$ and 0.485 for $I_L = -10A$ respectively. It has to be noted the small deviation in duty cycle between the two operating modes. This effect is produced by the voltage drop across the converter parasitic resistances and the batteries dynamic resistances.

TABLE I
Converter Operation Modes

Boost Mode		Buck Mode
d	=	$1-d$
$1-d$	=	d
A_1	=	A_2
A_2	=	A_1
B_1	=	B_2
B_2	=	B_1
A	=	A
B	=	B

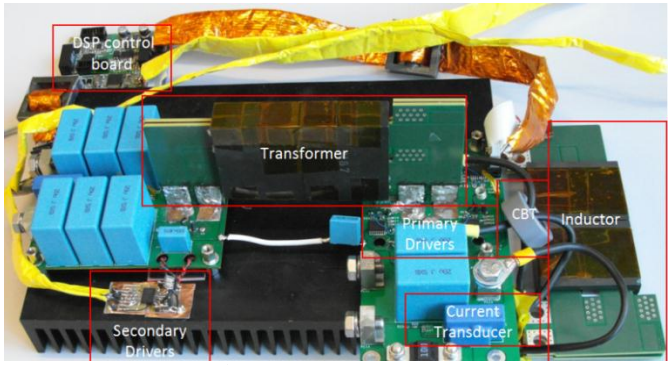

Fig. 7. Converter prototype.

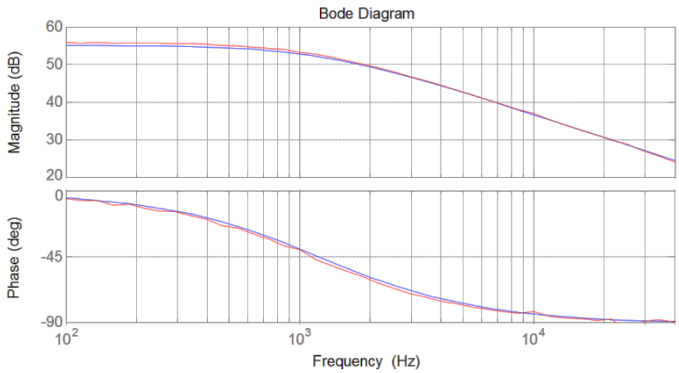

Fig. 8. Calculated (blue) and simulated (red) duty cycle-to-inductor current transfer function boost mode.

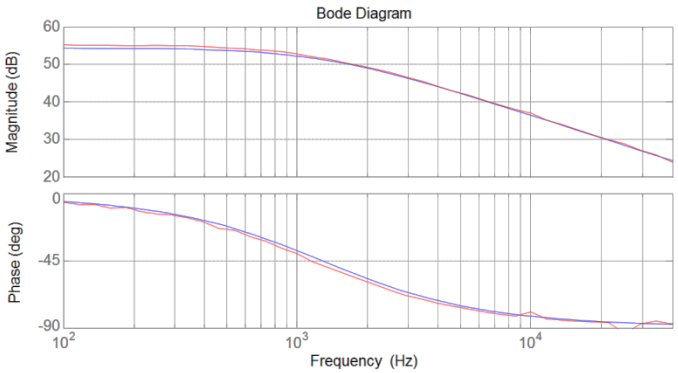

Fig. 9. Calculated (blue) and simulated (red) duty cycle-to-inductor current transfer function buck mode.

TABLE II
PARAMETERS OF THE CONVERTER

Battery A open circuit Voltage	$36V$
Battery B open circuit Voltage	$48V$
Transformer turn ratio	1:3
Inductor	13.5 μH
Transformer and inductor core material	Ferrite 3F3
Capacitor A	40 μH
Capacitor B	120 μH
Switches M1-M8	IPA075N15N3 G
Switches M9-M12	FDH055N15A
Switching frequency	50 kHz
Battery A dynamic resistance	60 $m\Omega$ @ 1kHz
Battery B dynamic resistance	80 $m\Omega$ @ 1kHz

TABLE III
CONVERTER PARASITIC RESISTANCES

r_L	3.9 $m\Omega$
r_{MP}	7.5 $m\Omega$
r_p	3.5 $m\Omega$
r_S	0.4 $m\Omega$
r_{MS}	5.9 $m\Omega$
r_{esrA}	3.15 $m\Omega$
r_{esrB}	1.1 $m\Omega$

It is important to note that for calculating the dc operating point, the battery terminal voltage will change as a function of the current direction and magnitude as well as the battery state of charge (SOC). As presented in [8], the battery can be modeled as a dependent voltage source in series with the battery dynamic resistance. True understanding of the changes in the terminal voltages is possible through accurate modeling of the battery with capacitance-like effects of the battery internal chemistry, which is beyond the scope of this work. In this paper, as shown in Table IV, the battery terminal voltages are measured at the desired operating conditions, and these values are used in the model to calculate the converter dc operating point. The converter loop measurements are performed for both operating modes with a dc power supply as the input source to the converter and the corresponding battery bank as the converter load. The power supply output resistance is assumed to be negligible at the frequencies of interest. Moreover, it should to be noticed that the measured battery terminal voltages already include the voltage drop across the battery dynamic resistances.

TABLE IV
CONVERTER STEADY OPERATING CONDITIONS

Boost Mode	Buck Mode
$V_G = 33.6\,V$	$V_{BatA} = 41\,V$
$V_{BatB} = 56.1\,V$	$V_G = 48\,V$
$I_L = 10\,A$	$I_L = -10\,A$
$d = 0.604$	$d = 0.422$

Converter current control loop has been closed inserting an integrator and a zero in the DSP before the converter low frequency pole. Although the converter plant transfer function is the same regardless of the current direction, different controllers have been used for boost and buck operation modes. This is due to the fact that the converter dc operating point is changed due to the battery terminal voltage being dependent on the current direction, which affects the converter transfer function. The compensation gain has been adjusted for a loop crossover frequency of 1 kHz for both operating modes.

Fig. 10 presents a measurement of the converter steady state waveforms. Fig. 11 and Fig. 12 show the calculated and measured converter loop gain and phase plots. The calculated model includes the controller transfer function implemented inside the DSP with the delays of sampling, algorithm calculation and PWM reconstruction, as well as the signal conditioning amplifier transfer function.

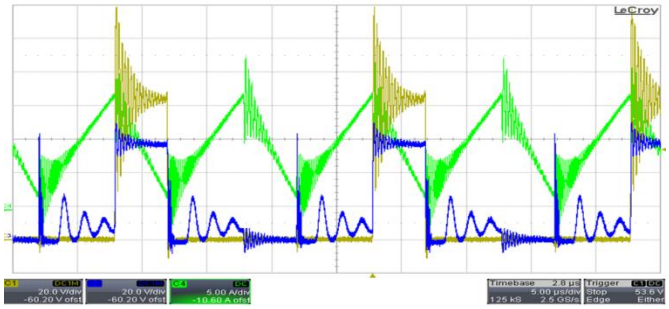

Fig. 10. Inductor current (green, 5A/div) with low voltage side (light brown, 20V/div) and high voltage side (blue, 20V/div) drain to source voltage waveforms during steady state operation. Time scale: 5µs/div.

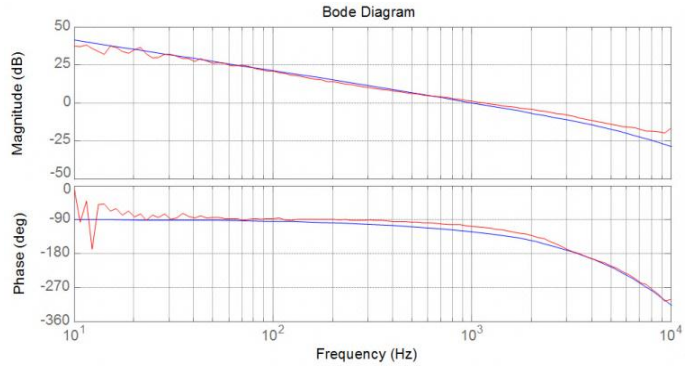

Fig. 11. Calculated (blue trace) and measured (red trace) open loop transfer function boost mode.

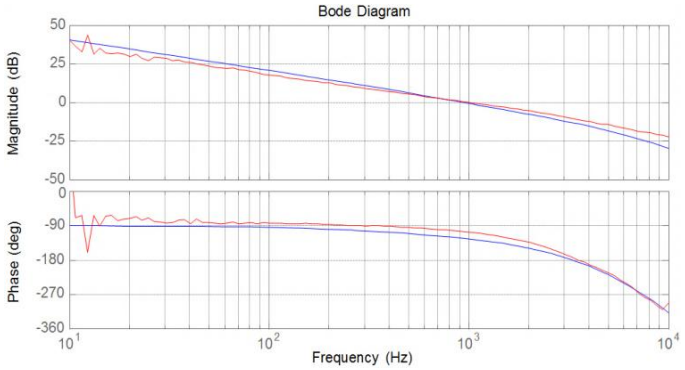

Fig. 12. . Calculated (blue trace) and measured (red trace) open loop transfer function buck mode.

The startup procedure of the converter with batteries in both sides is a complicated task. The implemented soft start function is able to turn on the converter in both directions without any additional circuitry.

While working with batteries, the duty cycle to inductor current transfer function has a larger gain compared to a pure resistive load for the same power level, meaning that the inductor current is very sensitive to small duty cycle perturbations in case of battery applications. The converter has to be started with minimum duty cycle without using synchronous rectification. Otherwise, starting with minimum duty cycle on one side will correspond to maximum duty cycle on the other side, creating an uncontrolled amount of initial current flow in the incorrect direction during converter startup. To avoid this situation, the converter should first be started by raising the current reference up to a certain startup current level. This current level has to be big enough to ensure CCM operation of the converter, otherwise, if the synchronous rectification is initiated, the duty cycle to inductor current transfer function will present a difference in dynamic behavior between DCM and CCM operation resulting in an uncontrolled current increase until the control loop manages to compensate the error.

Once the current trough the inductor has reached the desired level which ensures CCM operation, synchronous rectification can be started. At this point, the duty cycle for the synchronous MOSFETs is increased very slowly from zero to the final value calculated by the control law. This progressive introduction of the synchronous rectification avoids the current level to change again because of the difference in conduction resistance between the MOSFETs and the body diodes (used during normal rectification) that will affect the converter steady state conditions. Once the synchronous rectification has been introduced, the final step is to increase the reference value up to the desired final current level. This soft start procedure aims to remove unnecessary current and voltage stress from the switches at the start up increasing the converter reliability. The flow diagram of the proposed soft start procedure is presented in Fig. 13.

Fig. 14 shows the detailed startup sequence where the converter input current on the low voltage side together with the gate waveforms of the MOSFETs can be observed. Fig. 15 shows four current direction change events where the current change transition time has been adjusted to 100 ms.

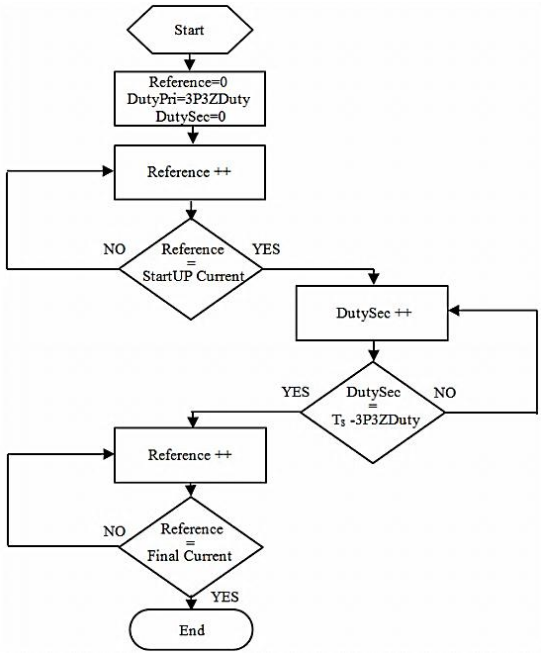

Fig. 13. Converter soft start flow diagram.

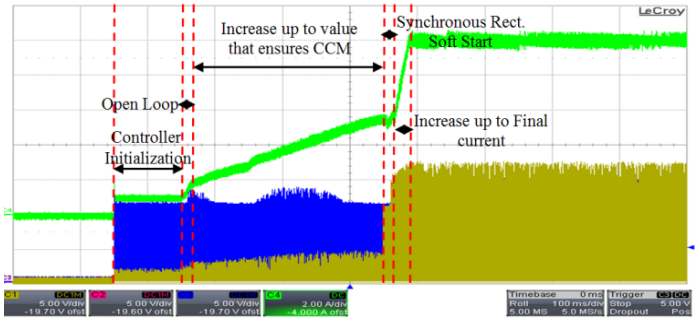

Fig. 14. Converter gradual soft start with two level inductor current reference change (green, 2A/div). Low voltage side MOSFETs gate waveform (blue, 5V/div) and high voltage side MOSFETs gate waveform (light brown, 5V/div.)Time scale: 100ms/div

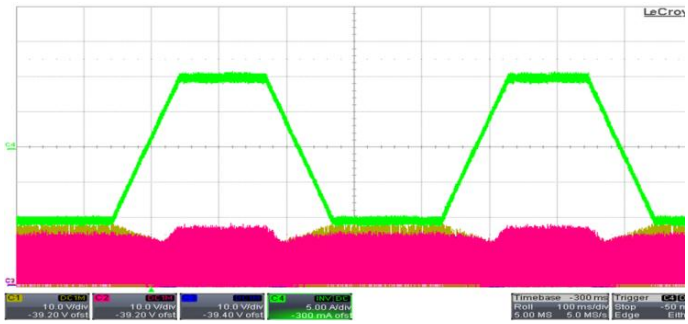

Fig. 15. Inductor current direction change with a defined ramp (5A/div. Time scale: 300ms/div).

IV. CONCLUSIONS

Bidirectional operation has been achieved by implementing synchronous rectification for primary parallel isolated boost converter (PPBIC). The converter dynamic model has been shown to be the same independent of the power flow direction, but two different controllers have been used in this experiment to compensate the converter steady state operating point variation due to the current dependence of the battery terminal voltage. Converter safe startup with batteries on both sides regarding component stress is a non-trivial situation. The implemented DSP startup procedure has proved that a soft start control of the current can be obtained and operation of the converter without any additional startup circuitry can be achieved.

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Appendix A5

[A5] **G. Sen**, Z. Ouyang, O. C. Thomsen, M. A. E. Andersen, L. Møller, "A high efficient integrated planar transformer for primary-parallel isolated boost converters," in Proc. ECCE 2010 (**Published**).

A High Efficient Integrated Planar Transformer for Primary-Parallel Isolated Boost Converters

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***Abstract* -- A simple, easy to manufacture and high efficient integrated planar transformer design approach for primary parallel isolated boost converters is presented. Utilizing the same phase flux flow, transformers are integrated, reducing the total ferrite volume and core loss for the same peak flux density. Number of turns is minimized for easy manufacturing by cascade placement of planar cores increasing the effective cross-sectional area. AC losses in the windings as well as the leakage inductance of the transformer are kept low by extensive interleaving of the primary and secondary turns. The idea of transformer integration is further extended to multiple primary power stages using modular geometry of the planar core, further reducing the core loss and allowing a higher power density. To verify the validity of the design approach, a 4-kW prototype converter with two primary power stages is implemented for a fuel cell fed battery charger application with 50-110 V input and 65-105 V output. Input inductors are coupled for current sharing, eliminating the use of current sharing transformers. An efficiency of 94% is achieved during nominal operating condition where the input is 70-V and the output is 84-V.**

***Index Terms*—planar integrated magnetics, coupled inductor, isolated boost converter, fuel cell.**

I. INTRODUCTION

Traction drive systems based on fuel cells and batteries require the dc-dc converter components to be selected for a wide range of input and output voltages depending on the fuel cell current and battery state-of-charge. This requirement limits the efficiency compared to a converter optimized around an operating point since the components have to be selected to cover the limits. So the dc-dc converter should be designed carefully to compensate for this situation [1].

Transformer design is a critical stage in high performance dc-dc converter design. In isolated boost converter applications, leakage inductance of the transformer should be minimized as well as the ac resistance since it causes spikes on the primary switch voltages increasing the inductive clamp losses [2]. Planar transformers have unique advantages in terms of increased power density, better cooling capability, modularity and manufacturing simplicity which make them attractive for high current dc-dc converter applications [3], [10]. In [4] and [5] integrated planar transformers for dc-dc converters have been studied. Improvements of AC resistance in transformer design are presented in [7], [8] and [9]. Also optimal design of transformers in high power, high frequency applications is mentioned in [11], [12] and [15].

Recently, significant achievements have been obtained in simple, low cost and high performance paralleling of converters for handling high currents in fuel cell applications which are presented in [13] and [14].

In this paper a new approach in transformer design for primary-parallel secondary-series isolated boost converters is presented. The idea is verified by simulation and experimental results.

II. PRIMARY PARALLEL ISOLATED BOOST CONVERTER

Boost derived topologies are preferred in fuel cell applications due to their low input current ripple. Fig.1 shows a primary parallel isolated boost derived topology suitable for handling high input currents for fuel cell applications. The dc current is forced to be equal in both primary stages by the series secondary connection of the two transformers. In order to compensate for the non-zero differential voltages in the two power stages that may occur due to gate signaling delays or parameter mismatches, a direct coupled input inductor is used, instead of a current sharing transformer. This coupled inductor divides the input current into two parts reducing the conduction losses and integrating two windings into a single core with a greater equivalent inductance.

In this topology, primary power stages share the same control signals with same phase switching sequence for the corresponding switches which allows a simpler control. Output rectification unit as well as input and output filters are common to both of the primary stages. Details of this topology and basic waveforms are presented in [2] and [13].

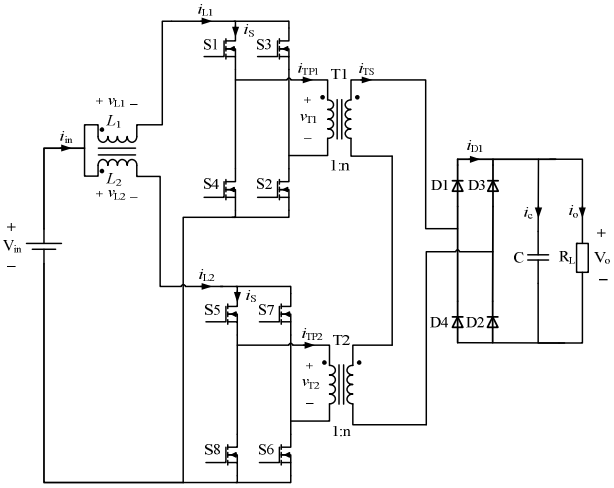

Fig. 1. Primary parallel isolated boost converter with coupled inductors for current sharing

Transformers T_1 and T_2 have the same number of turns with the same core size and material. Since the ac current sharing is ensured by the input coupled inductor, the same flux flows in both transformer cores. If it would be possible to wind both of the windings into the same core, they would produce the same peak flux density which would correspond to half the core loss since the total volume of ferrite is halved. But this method is not practical for standard E-cores due to the limited winding space; however it is possible to be achieved using planar E- cores by utilizing their modularity.

III. TRANSFORMER DESIGN

This section presents the new integrated planar transformer designed for the primary parallel isolated boost converter in Fig. 1, based on the arguments in the previous section. The new design provides higher power density, lower cost and higher efficiency compared to two separate transformers with the same core type. Planar structure also allows PCB windings to be used which make the manufacturing simpler and cheaper considering volume production. Also it allows easier realization for the interleaved winding arrangement.

A. Winding arrangement

Winding losses in transformers increase dramatically with increasing frequency due to skin and proximity effects. Based on Dowell's assumptions and the general field solutions for the distribution of current density in a single layer of an infinitely long foil conductor, the expression for AC resistance of a certain layer can be derived as in [6] and [9],

$$R_{ac,m} = R_{dc,m} \cdot \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2 \cdot \frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right] \quad (1)$$

where ξ is defined as

$$\xi = \frac{h}{\delta} \quad (2)$$

and δ is the skin depth for a specific frequency, which is given by

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}} \quad (3)$$

m is defined as

$$m = \frac{F(h)}{F(h) - F(0)} \quad (4)$$

where $F(0)$ and $F(h)$ are Magneto Motive Forces (MMF) at the limits of a layer as shown in Fig. 2. The first term in equation (1) describes the skin effect and the second term represents the proximity effect. The proximity effect loss in a multilayer winding, may strongly dominate the skin effect loss if the value of m increases which is related to the winding arrangement. Interleaving transformer windings can reduce the proximity loss significantly (decrease m) when the primary and secondary currents are in phase. In this research 3:1 turns ratio is used for each transformer. There are 3 turns in series on the primary side; and a single turn with four layers in parallel on the secondary side to sustain high current. Fig. 2 shows the MMF distributions along the vertical direction for the interleaved arrangement of the designed transformer. Fig. 3 shows the AC resistance relative to the DC resistance in a layer having a thickness equal to the skin depth. The layer thickness can be selected for minimizing the AC losses according to the value of m. In this case switching frequency is 50-kHz and 0.14-mm PCB layer thickness has been chosen for each layer.

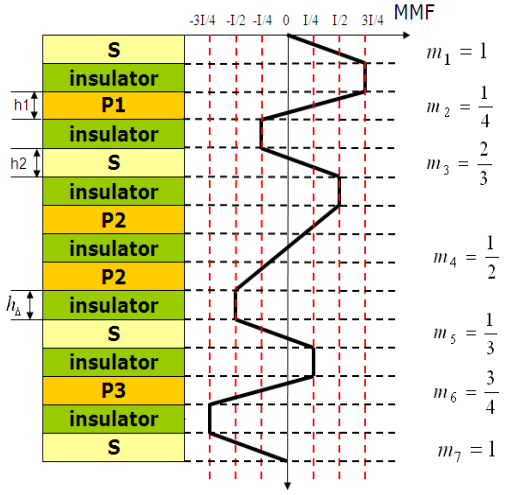

Fig.2. MMF distributions for interleaved arrangement for the proposed transformer.

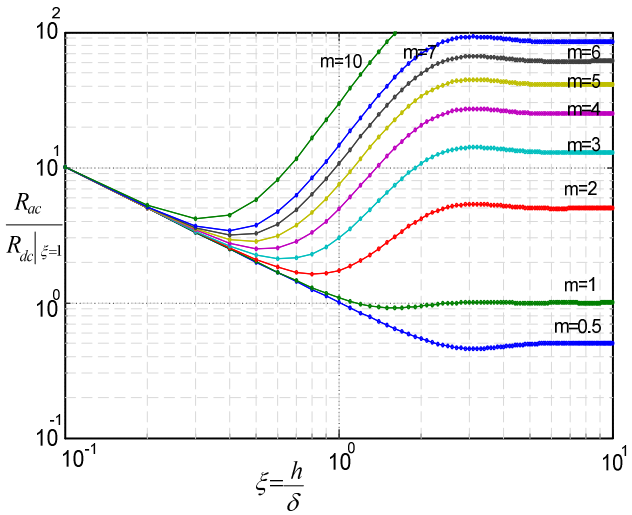

Fig. 3. AC resistance relative to dc resistance in a layer with different values of thickness over skin depth.

B. Cascaded structure

Proposed integrated planar transformer has been built using a cascaded core structure to minimize the number of turns. Fig. 4 shows the construction of each transformer with two planar E-cores placed side-by-side which adds up to four

E-cores and two I-cores for the whole integrated structure. Increased cross-section by cascading avoids saturation and reduces core loss when the same number of turns is used in a non-cascaded (single) core construction. According to Faraday's law peak-to-peak flux density is,

$$\Delta B = \frac{V \cdot \Delta t}{N \cdot A_e} \tag{5}$$

where N, A_e are the number of turns and the cross-section of centre leg of the core respectively. $V \cdot \Delta t$ is volt-seconds applied to the transformers. Core loss of a transformer depends on the material that the core is made from, the switching frequency, the flux density, and the volume of the core. The Steinmetz Equation can be used to compute the core loss given in equation (6),

$$P = K \cdot f^{\alpha} \cdot (\Delta B/2)^{\beta} \cdot V_e \tag{6}$$

K, α and β are constants that are provided by the manufacturer or can be calculated from the curves of a specific core loss data. Combining equation (5) with equation (6) and having the ratio of the two different cases,

$$P_{cc} = 2^{1-\beta} \cdot P_{co} \tag{7}$$

where P_{cc} and P_{co} represent the core losses of 2 cores cascaded transformer and a single core transformer with the same number of turns, respectively. Generally β is more than 1, therefore the cascaded transformer has lower core loss according to eqn. (7). It has to be noted that winding loss will be sacrificed due to longer turn lengths. In this work 3F3 core material is used which has β approximately equal to 2.6.

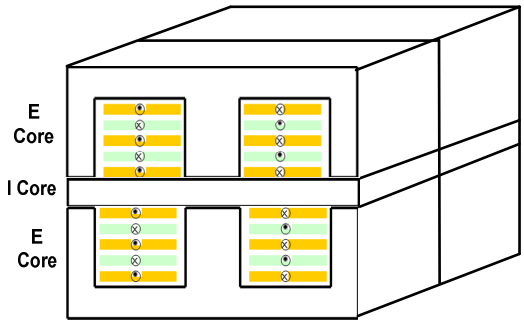

Fig.4. Two transformers in E-I-E integration.

C. Magnetics Integration

In order to reduce the transformer footprint area and increase the converter power density, transformers T_1 and T_2 in Fig. 1 are integrated utilizing the modular flexibility of the planar cores. The new structure is shown in Fig. 4. Two integrated transformers are located on top of each other. Two cascaded I-cores are shared in the centre part. The symmetrical windings of the two transformers will allow the flux in the I-cores to be cancelled which reduce the core loss. 3D FEA simulation result in Fig.7 shows the flux in I-core (centre part) to be almost zero. More transformers can be integrated based on this principle which will further reduce the overall core loss since the flux will only flow in the outer core sections (Fig. 5).

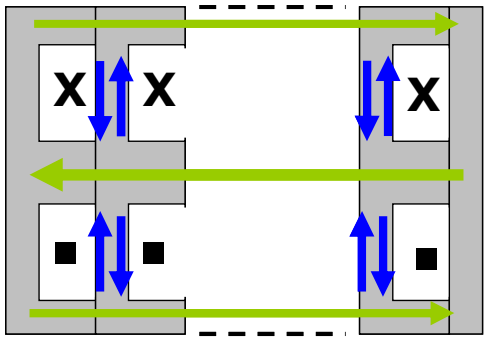

Fig.5. Integration of n number of transformers with main flux lines (green) and cancelled flux lines (blue).

D. Magnetic reluctance model

Fig.6 shows the magnetic reluctance model of the integrated structure where R_1 and R_2 are the reluctances of outer legs of E-core and half I-core respectively. Similarly R_c represents the reluctance of the center leg of E-core.

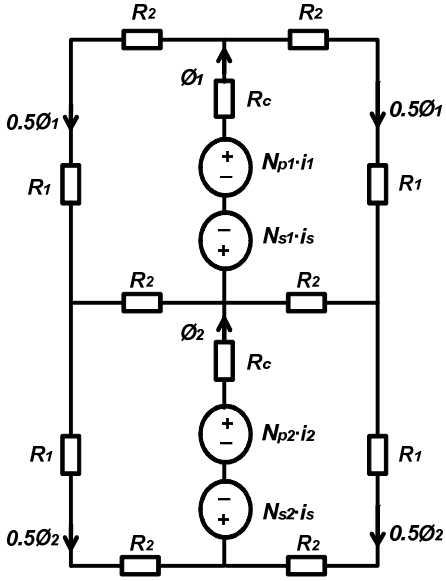

Fig.6. Reluctance model of the integrated transformer.

Based on the equivalent magnetic model in Fig.6, major flux directions can be determined. In order to calculate the magnetizing inductance of the integrated module referred to the secondary side, the equations (8) and (9) can be obtained assuming the primary windings to be shorted,

$$N_{s1} \cdot i_{ms} = \phi_1 \cdot R_c + 0.5 \cdot \phi_1 \cdot (R_1 + R_2) + 0.5 \cdot (\phi_1 - \phi_2) \cdot R_2 \tag{8}$$

$$N_{s2} \cdot i_{ms} = \phi_2 \cdot R_c + 0.5 \cdot \phi_2 \cdot (R_1 + R_2) + 0.5 \cdot (\phi_2 - \phi_1) \cdot R_2 \tag{9}$$

where i_{ms} is the magnetizing current referred to the secondary side. Since the two transformers, T_1 and T_2 are identical,

$Ø_1$=$Ø_2$ and N_{s1}=N_{s2} can be used. Therefore, the magnetizing inductance of each transformer in the integrated module referred to the secondary side can be derived as,

$$L_m^{'} = \frac{2N_s^2}{2R_c + R_1 + R_2} \tag{10}$$

The magnetizing inductance of a single separated transformer would have the following expression,

$$L_m = \frac{2N_s^2}{2R_c + R_1 + 2R_2} \tag{11}$$

Comparing magnetizing inductances of the integrated and separated transformers using (10) and (11), $L_m^{'} > L_m$ can be observed which means the integrated transformers have higher magnetizing inductance compared to the separated case. This is because of the fact that the flux cancellation occurs in the shared I-core effectively reducing the length of flux path. Higher magnetizing inductance reduces the magnetizing current which helps in the current stress over the components.

E. Measurement results

Fig.8 and Fig.9 show the leakage inductance and AC resistance measurement results of the designed single transformer and the integrated transformers respectively using PSM1735 impedance analyzer. For the single transformer, the leakage inductance is 25.76-nH and the AC resistance is 2.50-mΩ referred to secondary side when the frequency is 50-kHz. This measurement has been taken by shorting the primary side and connecting the secondary terminals to the impedance analyzer. For the integrated transformers, the total leakage inductance referred to the secondary side is 40.25-nH and the total AC resistance is 5.53-mΩ. Fig.10 shows the measurement results of magnetizing inductances. Results confirm the previous analysis that the total magnetizing inductance of the two integrated transformers is greater than that of the two series connected separated transformers.

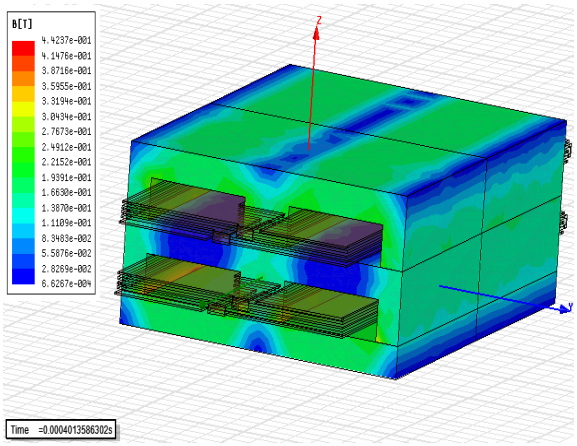

Fig.7. 3D FEA simulation for integrated transformers

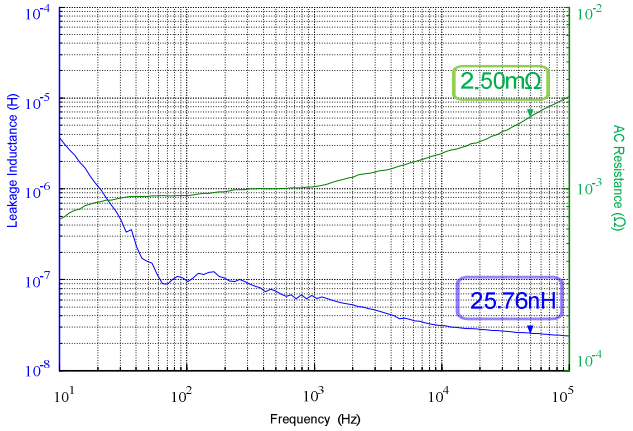

Fig.8. Measurement results of ac resistance and leakage inductance of a single transformer referred to the secondary side

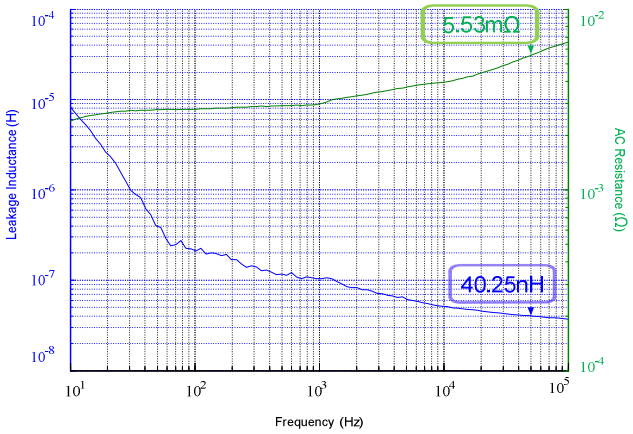

Fig.9. Measurement results of ac resistance and leakage inductance referred to the secondary side for the deigned integrated transformer

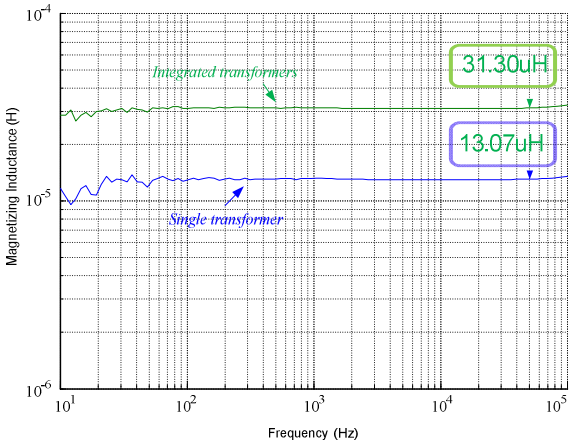

Fig.10. Measurement results of magnetizing inductances of both single and integrated transformers referred to secondary side

Table I summarizes the design parameters for the integrated transformer. Each PCB winding has 8 layers where 4 layers used in parallel for the single secondary turn and the remaining 4 layers are used for three primary turns with one of the turns used two layers in parallel.

Table I
Design parameters for the integrated transformers

Parameters	Values
Number of turns in primary of T_1 (N_{p1})	3
Number of turns in primary of T_2 (N_{p2})	3
Turns ratio of each transformer	3:1
Planar Core type	EILP 64
Core material	3F3
Number of layers of PCB winding	8
Copper thickness for each layer of PCB winding	4 OZ (140um)
AC resistance referring to the secondary side	5.53mΩ
Leakage inductance referring to the secondary side	40.25 nH
Magnetizing inductance referring to the secondary side	31.3 uH

IV. Experimental Results

A 4-kW prototype converter has been built to verify the new integrated transformer design approach. Input voltage is between 50-110 V and output voltage is 65-105 V. Primary switches are IRF4668, 200-V, 8-mΩ power MOSFETs from International Rectifier. Output rectification is handled by 80CPQ150 schottky diodes with 0.82-V forward voltage drop.

The two integrated transformers are implemented using four E-64 and two I-64 planar cores with 3F3 material. The primary and secondary windings are implemented using PCB windings with 0.14-mm layer thickness.

The coupled input inductor is wound on a KoolMμ 6527E040 core with 0.4-mm copper foil having 12 turns in each winding. In order to reduce the AC conduction losses of the inductor, 0.1 mm copper foil is used for a parallel inner winding with the same number of turns giving a lower AC resistance. This two parallel winding approach helps in providing a low AC resistance and leakage inductance path for the inductor current ripple.

IRS2110 high and low side gate drivers are used in the gate driver circuit together with ISO722C capacitive digital isolators for control signal protection. Open loop control signals are produced by TMS28027 DSP from Texas Instruments. Fig. 11 shows the implemented prototype with all the switches mounted to a heat sink beneath the converter. Output is filtered by six 20-uF and two 820-nF film capacitors placed very close to the rectifiers for minimizing the ac loop.

Converter waveforms are presented in Figs. 12 and 13. Coupled inductor current waveforms, i_{L1} and i_{L2}, are observed to be very close in average value confirming the current sharing function of the coupled inductor. An efficiency of 94% has been observed with 70-V input voltage, 84-V output voltage and 3-kW input power.

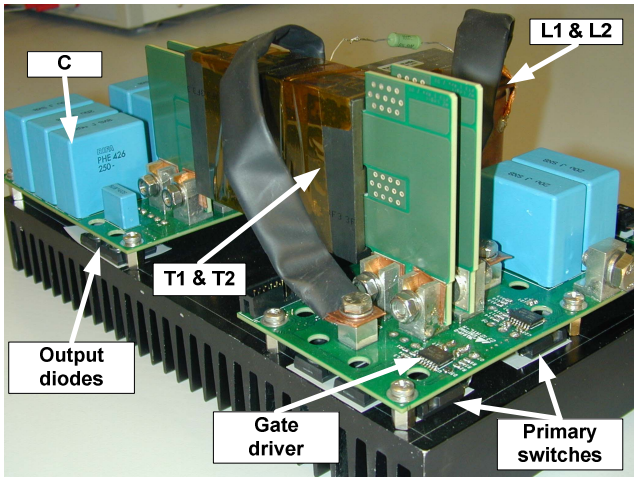

Fig. 11. Experimental prototype of integrated transformer primary parallel isolated boost converter

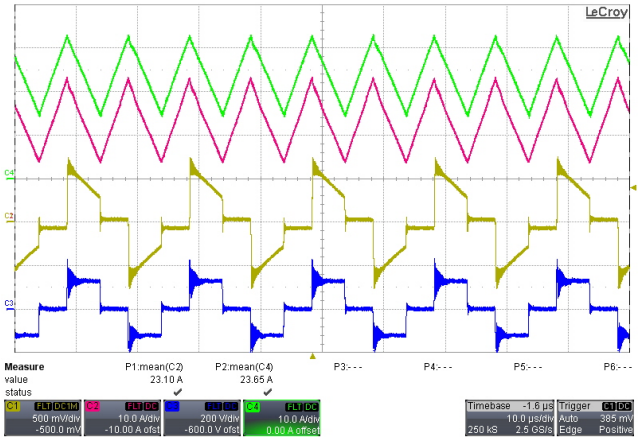

Fig. 12. Converter waveforms (V_{in}: 70V, V_o: 84V). Ch4: i_{L2} (10A/div), Ch2: i_{L1} (10A/div), Ch1: i_{TP1} (25A/div), Ch3: V_{T1} (200V/div).

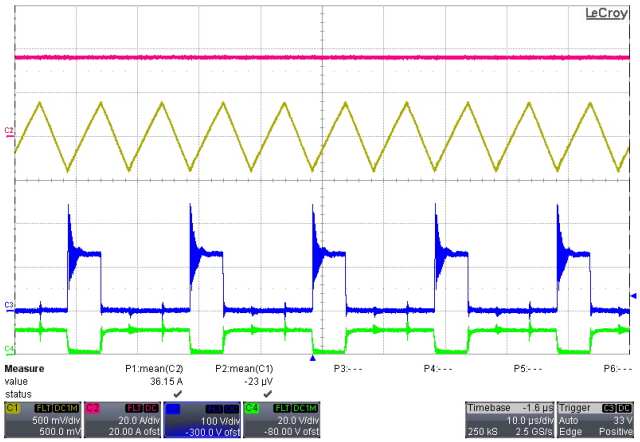

Fig. 13. Converter waveforms (V_{in}: 70V, V_o: 84V). Ch2: i_O (20A/div), Ch1: i_{in} ripple (25A/div), Ch3: V_{DS} of S2 (100V/div), Ch4: V_{GS} of S_2 (20V/div).

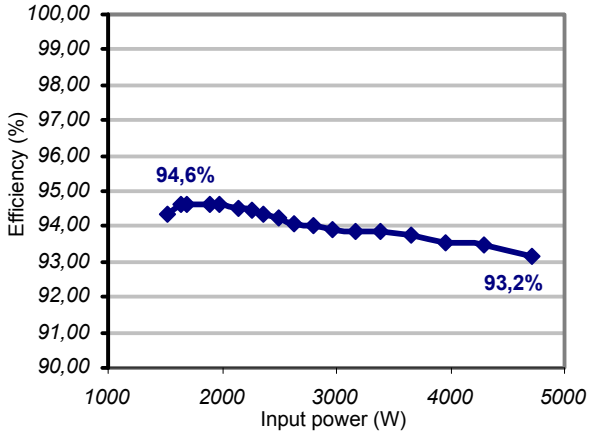

Fig. 14. Converter efficiency(V_{in}: 70V, V_o: 84V).

V. CONCLUSION

A new method is proposed for transformer integration in primary parallel isolated boost converters. Utilizing the symmetry and in-phase switching in each power stage, cores of the transformers have been integrated sharing the same flux. Any small difference in flux generated by each integrated transformer is compensated by the "I" cores placed in between. Number of turns is minimized by cascade placement of E cores per transformer, decreasing the effective cross sectional area. This simplifies manufacturing and decreases the winding losses. Extensive interleaving has been used for minimizing ac resistance and leakage inductance. The new integration method has been tested in a 4-kW prototype.

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Appendix A6

[A6] **G. Sen**, Z. Ouyang, O. C. Thomsen, M. A. E. Andersen, L. Møller, "Integrated current balancing transformer for primary parallel isolated boost converter," in Proc. EPE 2011 (**Published**).

Integrated Current Balancing Transformer for Primary Parallel Isolated Boost Converter

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Keywords

«DC power supply», «integrated passive components», «passive components»

Abstract

A simple, PCB compatible integrated solution is proposed for the current balancing requirement of the primary parallel isolated boost converter (PPIBC). Input inductor and the current balancing transformer are merged into the same core, which reduces the number of components allowing a cheaper and more compact solution. Gyrator-Capacitor modeling technique has been used, providing an easy way for understanding integrated magnetic structures. Proposed idea has been verified by simulation and experimental results.

Introduction

Planar magnetics have unique advantages in terms of increased power density, better cooling capability, modularity and manufacturing simplicity [1], [5]-[9]. Recently, PPIBC has been proposed as an attractive, high efficient solution for high input current, step up DC/DC applications [4] and integrated planar technology has been successfully applied to this topology [2]. In this paper, a new approach in implementing the input inductor and the current balancing transformer of PPIBC in the same core is presented.

Primary Parallel Isolated Boost Converter

Fig. 1 shows PPIBC topology suitable for handling high input currents for fuel cell applications. The dc current is forced to be equal in both primary stages by the series secondary connection of the two transformers. Primary switches share the same control signals with the same phase switching sequence which allows a simple control. Output rectification unit as well as input and output filters are common to both primary stages. Details of this topology and basic waveforms are presented in [4].

The input inductor in Fig. 1 serves as an energy storage element for both primary power stages. As long as switches S1, S2, S3, S4 and S5, S6, S7, S8 work in the same pattern (Fig. 2a), the inductor current will be shared equally by the two full bridges. In case of a mismatch in switching, the current sharing transformer (effectively an inverse coupled inductor) in series with the input inductor shows high impedance in the differential path which limits the rate of change of the differential current (Fig. 2b). This will force the ac components of the currents in the two branches to be equal depending on the inductor value in the differential path. The simulation results in Fig.3 show the current balancing transformer suppressing the ac differences in the currents in each branch.

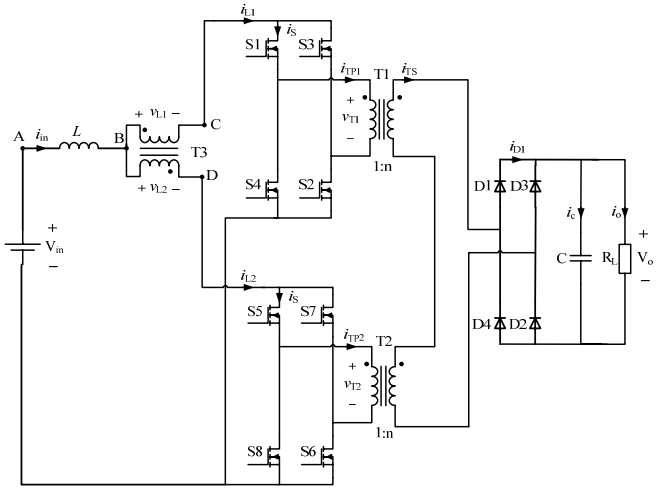


Fig. 1: Primary parallel isolated boost converter with current balancing transformer

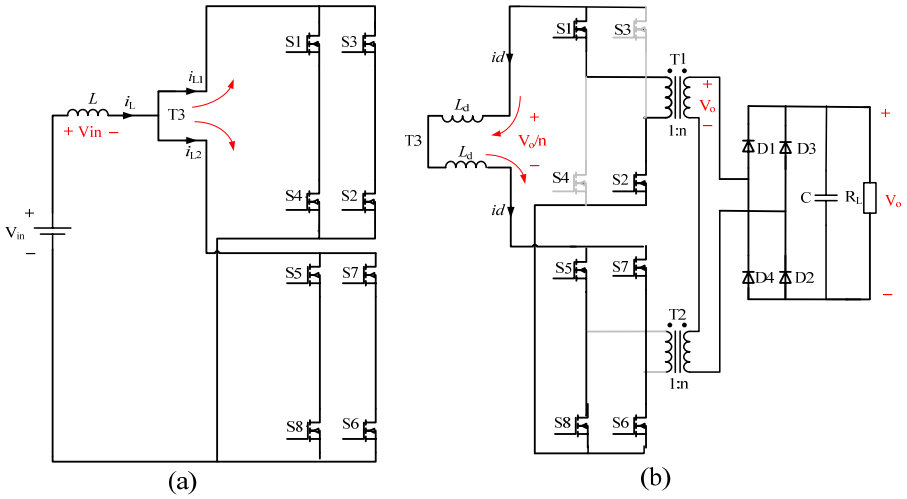


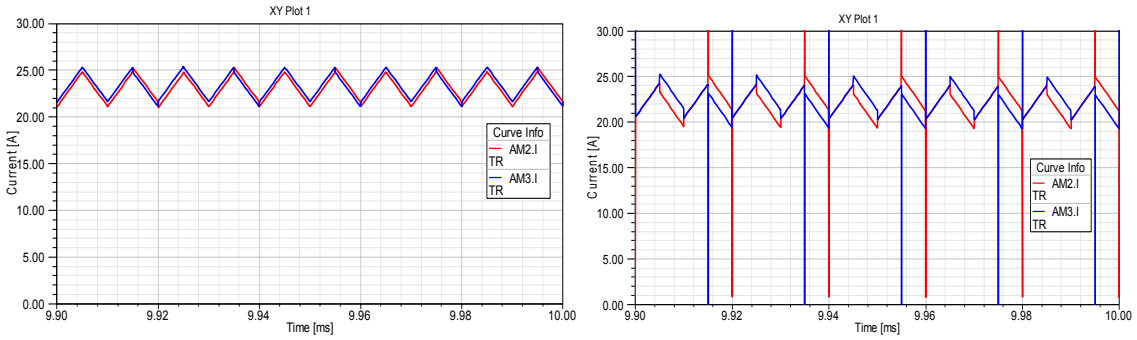
Fig. 2: (a) Forward current path during boosting (b) differential current path during gate signal mismatch

In [4], the current balancing transformer is implemented as a planar based discrete component. However, considering the small mismatch times of the switches due to the propagation delays of the ICs and parasitic elements in the gate drive circuitry, the planar core of the discrete current balancing transformer is not being used during most of the switching period. This results in an inefficient use of the core. Therefore the idea of sharing a core with another magnetic element can be proposed.

Proposed Integrated Current Balancing Transformer

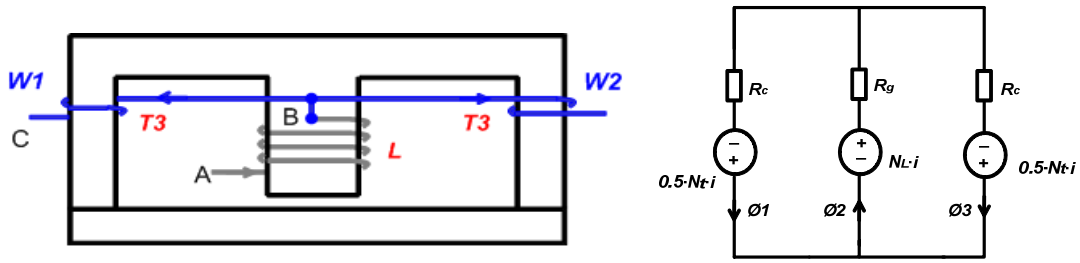
The proposed integrated structure is shown in Fig.4. Both center leg and outer legs of the core are being used. Corresponding circuit model is shown in Fig. 5. Additional windings on the outer legs are reverse coupled on the forward path and direct coupled in the differential path. The magnetic reluctance model is shown in Fig.4b, where N_t and N_L are the number of turns of the winding in the outer leg and the center leg respectively. R_c is the reluctance of the outer leg of the core and R_g represents the reluctance of the center leg. R_g is much bigger than R_c due to the air gap of the center leg. The flux equations using superposition principle can be obtained as,

$$0.5 \cdot N_t \cdot i - \Phi_1 \cdot R_c = N_L \cdot i - \Phi_2 \cdot R_g \;\&\; \Phi_2 = \Phi_1 + \Phi_3 \;\&\; \Phi_1 = \Phi_3 \qquad (1)$$



(a) Current balancing transformer used (b) No current balancing mechanism used

Fig. 3: Simulation results for currents flowing into each full bridge in Fig. 1.



(a) Proposed integration structure (b) Magnetic reluctance model

Fig. 4: Physical placement of the windings and basic modeling

According to Faraday's law, inductances corresponding to each leg can be obtained as,

$$L = \frac{N_L \cdot (N_t + N_L)}{R_g + R_c/2} \;\&\; L_c = L_{c1} = L_{c2} = \frac{N_t \cdot (N_t + N_L)}{R_g + R_c/2} \;\&\; L_d = \frac{(2N_t)^2}{2R_c} \tag{2}$$

The integrated solution has the advantage of eliminating the extra core for the current balancing transformer T3, reducing the cost and the volume of the converter. As shown in Fig. 5, additional inductances (L_{c1} and L_{c2}) are appearing in the forward path due to the direct coupling between L and T3 which reduces the input inductor current ripple. Differential inductances (Ld) in T3 depend on the reluctance of the outer loop of the core in Fig. 4a which does not contain any air gap. This low reluctance path allows for having low number of turns for a certain inductance in the outer leg.

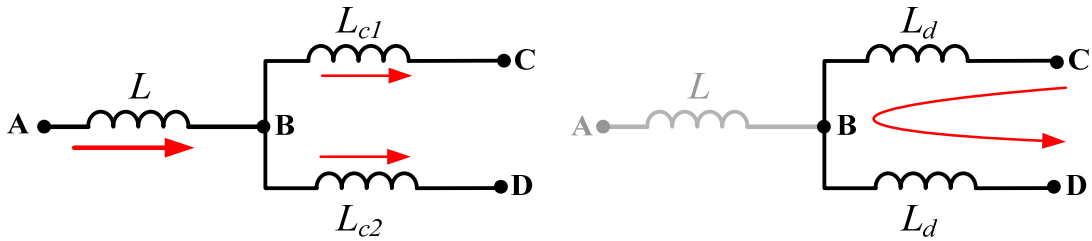


Fig. 5: Circuit models of the integrated structure in (a) forward and (b) differential path

G-C Modeling and FEA Simulation

Gyrator-Capacitor (G-C) modeling technique has been used in the literature especially for integrated magnetic design [10]-[12]. It is a simple and intuitive method which uses capacitance, representing the magnetic core permeance. This approach is compatible with the energy storing capability of a magnetic core, which can not be represented by the reluctance model. Fig. 6 shows the G-C model of the proposed integrated magnetic structure. The model consists of two parts: 1) magnetic part represented with electrical circuit elements (black), 2) electrical part composed of center leg and side leg windings (red).

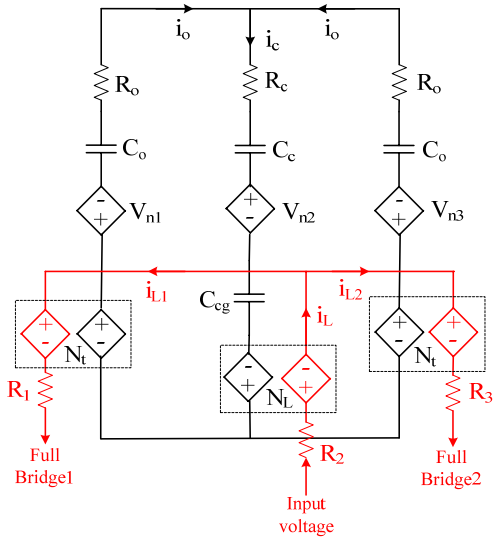


Fig. 6: (a) G-C model of the proposed integrated structure

The coupling points between the electrical and magnetic parts of the model are the current controlled voltage source pairs inside the dashed frames on each leg. The currents i_L, i_{L1} and i_{L2} in the windings are converted into MMFs represented as voltages in the magnetic circuit. The currents i_o and i_c flowing in the magnetic circuit represent the respective flux rates on the core legs which are converted into voltage drops on the windings depending on the number of turns (N_L and N_t). Capacitances C_o and C_c represent the permeances of the outer and center legs where the air gap permeance in the center leg is represented by C_{cg}. Resistances R_1, R_2 and R_3 are the winding resistances. Core loss in each leg can also be represented by the resistances R_o and R_c. Saturation of the core has been represented by the voltage controlled voltage sources V_{N1}, V_{N2} and V_{N3} for each leg. Details of model parameter calculations can be obtained from [10]-[11]. In order to verify the operation of the proposed integrated magnetic structure, the model in Fig. 6 has been simulated. The simulation results with and without outer leg windings are shown in Fig. 7. In Fig.7a center leg has four turns and each outer leg has two turns. On the other hand, Fig. 7b has six turns only in the center leg. The increase in the ripple current in Fig. 7a compared to Fig. 7b is the result of smaller number of turns in the center leg. Since the two outer leg inductances are in parallel in the forward path, effective inductance is reduced. This can be counted as a disadvantage of the method considering the same amount of copper and window area.

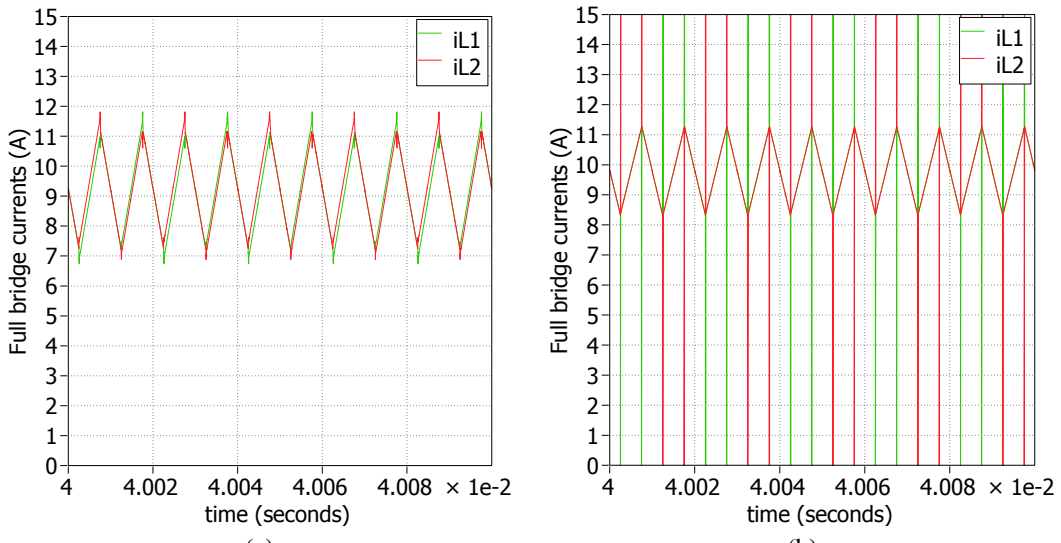


Fig. 7: Simulation of the G-C model: full bridge currents (a) with and (b) without outer leg windings

In order to see the details of the flux distribution in the core, FEA simulations have been carried out. Fig. 8 shows the results for two different cases of winding arrangement. The result in Fig. 8a has been obtained using the configuration in Fig. 4a, where the outer leg windings are reverse coupled with respect to each other, which results in a direct coupling with the winding in the center leg. Fig. 8b shows the case where the outer leg windings are direct coupled, which is included here to investigate as a possible mistake during the winding process. The unbalance of flux distribution and saturation are clearly observed in the latter case. This can be understood by considering the magnetic circuit in Fig. 4b. Here, if one of the outer leg MMF source polarities is reversed, a much bigger amount of flux is produced due to the low reluctance non-gapped outer path. It should be noted that the scales in Fig. 8a and Fig. 8b are not kept the same due to the relatively big difference in flux in both cases.

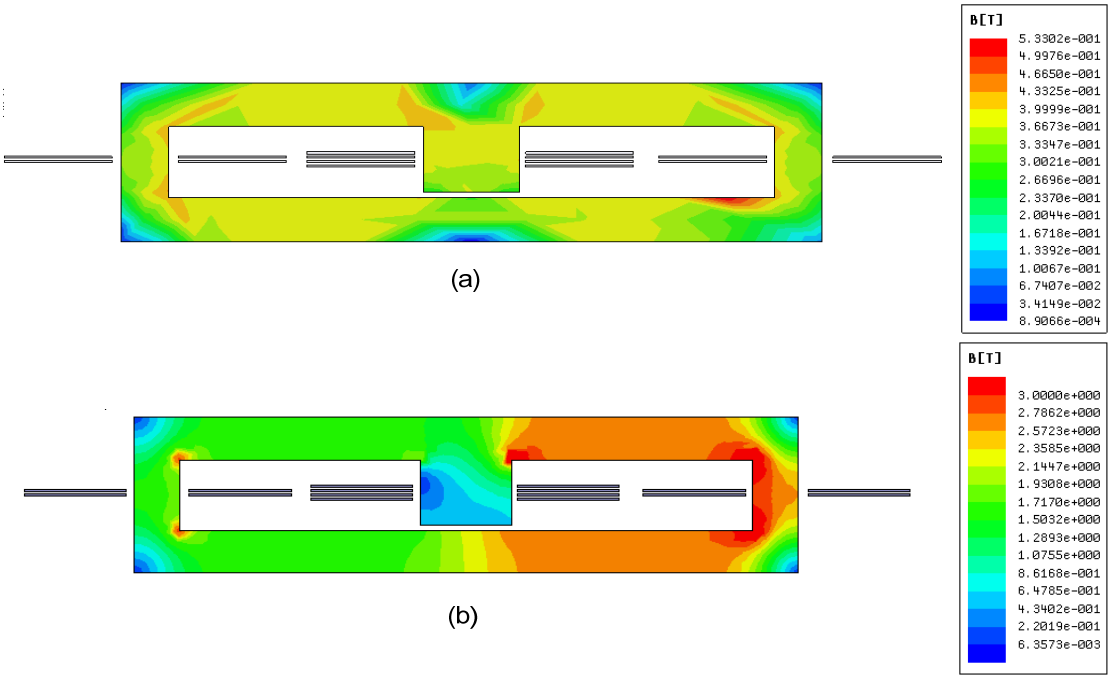
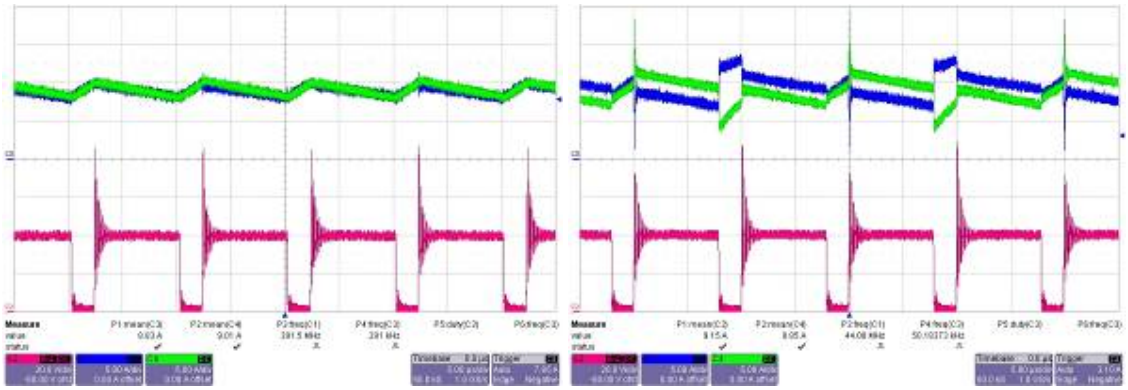


Fig. 8: Finite element analysis of the integrated structure a) with proper coupling of the outer leg windings (b) uneven flux distribution and saturation due to wrong coupling

Experimental Results

A 1kW converter with the integrated current balancing transformer has been built to verify the validity of the proposed idea of integration. Input voltage is between 20-50 V and output voltage is 170-200 V. Primary switches are IPA028N08N3, 80-V, 2.8-mΩ power MOSFETs from Infineon. Output rectification is handled by V30200C Schottky diodes with 0.65-V forward voltage drop. IRS2110 high and low side gate drivers are used in the gate driver circuit together with ISO722C capacitive digital isolators for control signal protection. The control signals are produced by a Texas Instruments TMS320F28027 DSP. Output is filtered by two 10-uF capacitors placed very close to the rectifiers for minimizing the ac loop. Converter waveforms are presented in Fig.9. In Fig. 9a, a small deviation occurs between the currents at the mismatch instants where Fig. 9b shows the clear unbalance with very high rate of change of the currents at the mismatch instants.

A picture of the experimental setup is given in Fig. 10. The integrated current balancing transformer is implemented with ELP58 cores with N87 material. The details of the windings can be seen in Fig. 11. Maximum efficiency of 96% has been observed with 40-V input voltage, 180-V output voltage and 800-W output power.



(a) (b)

Fig. 9: Experimental results for currents going into each full bridge in Fig. 1. (a) with and (b) without current balancing transformer

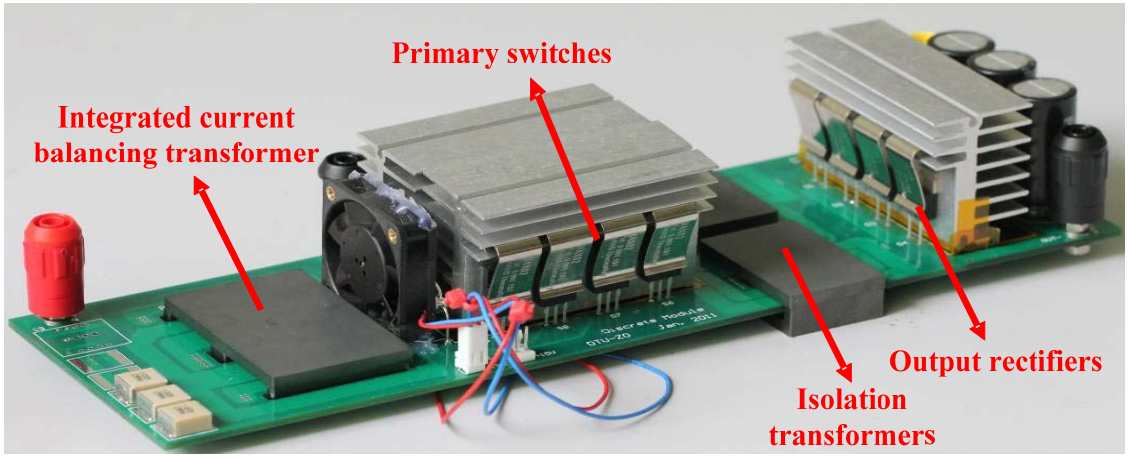


Fig. 10: Experimental prototype of PPIBC with integrated current balancing transformer

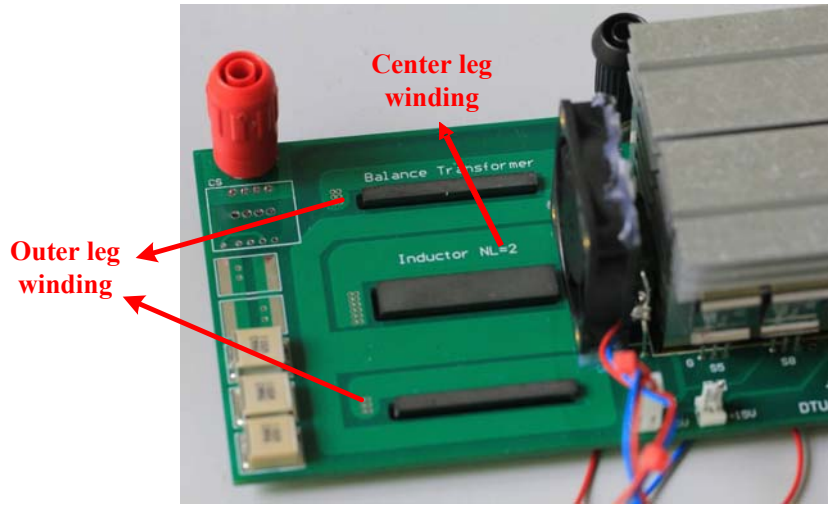


Fig. 11: Detailed view of the PCB tracks

 ISBN: 9789075815153

Conclusion

This work presents a new approach in implementation of the current balancing transformer for primary parallel isolated boost converter. Instead of using a separate core the current balancing transformer is implemented in the same core with the input inductor. This reduces the number of components and the number of terminations in the converter. The extra windings in the side legs of the integrated core provide additional inductance in the forward path as well as in the differential path. The new integrated design approach provides a high power density and higher efficiency alternative to the discrete design.

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Appendix A7

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Fully Integrated Planar Magnetics for Primary-Parallel Isolated Boost Converter

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***Abstract*- A high efficient planar integrated magnetics (PIM) design approach for primary parallel isolated boost converters is presented. All magnetic components in the converter including two input inductors and two transformers with primary-parallel and secondary-series windings are integrated into an E-I-E core geometry. Due to a low reluctance path provided by the shared I-core, the two transformers as well as the two input inductors can be integrated independently, reducing the total ferrite volume and core loss. AC losses in the windings and the leakage inductance of the transformer are kept low by interleaving the primary and secondary turns of the transformers. To verify the validity of the design approach, a 1-kW prototype converter with two primary power stages is implemented for a fuel cell fed battery charger application with 20-40 V input and 170-230 V output. An efficiency of 96% can be achieved during nominal operating conditions. Also experimental comparisons between the PIM module and two separate cases have been done in order to illustrate the advantages of the proposed method.**

I. INTRODUCTION

In order to meet the requirements of modern power electronics applications, magnetics integration with planar core has proven to be an effective means of reducing the converter size, the cost and increasing the converter efficiency [1]-[3]. Planar magnetics have unique advantages in terms of increased power density, better cooling capability, modularity and manufacturing simplicity as well as easy implementation of interleaved windings, which make them attractive for high current DC/DC converter applications [4]-[10].

In recent years, most of efforts in integrated magnetics (IM) focus on the current-doubler rectifier due to its suitability for low-output-voltage and high-output-current applications. Unlike the conventional magnetic integration focusing only on core integration, both core and winding integration can be realized in the current-doubler rectifier design, causing lower conduction loss and core loss. As a result, lower overall cost, size as well as higher efficiency can be obtained in the IM deign for current-doubler circuit [1]-[3], [9]. A 1-kW with 300~400-V input and 48-V output AHBC asymmetrical half-bridge PWM converter employing the integrated L–L–C–T module is constructed in [8]. Detailed suggestions are given of how one generic, integrated LCT component could be used to implement various resonant converter topologies by merely reconfiguring the external terminals of the integrated component [10]-[11]. An integrated transformer consisted of four step-down transformers wound on a single magnetic core for an interleaved four-phase forward converter has been proposed [12]. Since the steady-state inductor current ripples can be greatly reduced without comprising the transient response, coupled inductors with compact structure has been also paid attention in recent [13]-[15].

Nowadays, a new trend of magnetics design in power electronics is to reduce ac resistance and leakage inductance by using distributed magnetics [16], which functionally splits a large magnetic element into small magnetic element. A new very high efficiency 10 kW isolated R4 boost converter for low-voltage high-power fuel cell applications [17],[18] has illuminated its advantage due to their lower transformer turns ratio and parallel structure. Matrix transformers actually have such behaviors as well. Over 40% of the effective winding resistance and 20% leakage inductance can be reduced by Matrix transformers [19], making it very attractive for high current applications. However, increased numbers of components reduce power density of converters, as well as power efficiency in the light load due to higher core loss. Therefore, integration for the distributed magnetics becomes very important in order to solve these problems.

In this paper, a new approach to integrate magnetics design associated with all magnetic components for the primary-parallel isolated boost converter is presented. Two input boost inductors and two transformers are integrated into an E-I-E core geometry. The modeling of integrated structure is presented in Section III. The flux generated from each magnetic component can be partially cancelled in the PIM module, resulting in a lower core loss. Integrated transformers in this geometry have higher magnetizing inductance compared to the separated case, reducing current stress. AC losses in the windings and the leakage inductance of the transformers are kept low by interleaving the primary and secondary turns of the transformers. To verify the validity of the design approach, a 1-kW prototype converter with two primary power stages is implemented for a fuel cell fed battery charger application with 20-40 V input and 170-230 V output. An efficiency of 96% can be achieved during nominal operating conditions. In order to performance advantages of the method, experimental comparisons between the PIM module and two separate cases have been done, the results show the PIM module has a lower footprint as well as higher efficiencies can be achieved in both full load ranges and full input voltage ranges.

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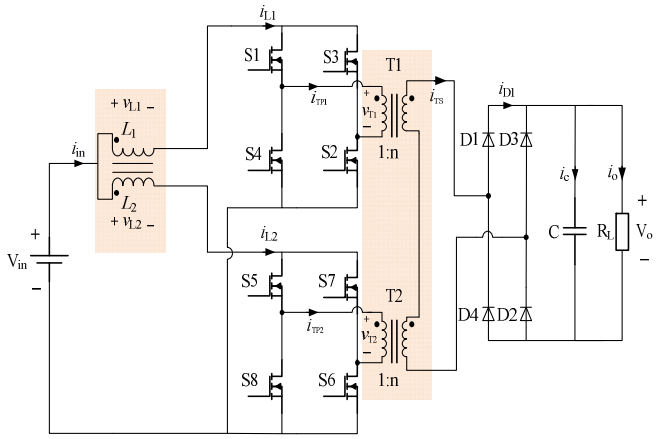

Fig. 1. Primary-parallel isolated boost converter with coupled inductors for current sharing.

II. PRIMARY-PARALLEL ISOLATED BOOST CONVERTER

Boost derived topologies are preferred in fuel cell applications due to their low input current ripple [20]. Fig.1 shows a primary-parallel isolated boost derived topology suitable for handling high input currents for fuel cell applications. Series connection of transformer secondary windings ensures current sharing during energy transfer cycle when power is transferred to output. In this topology, primary power stages share the same control signals with same phase switching sequence for the corresponding switches which allows a simpler control. Output rectification unit as well as input and output filters are common to both of the primary stages. The paralleling method splits a critical primary high-ac-current-loop into two smaller loops. Each of the smaller loops only need to switch half of the input current thereby achieving much faster current switching and thus higher conversion efficiency. Since the two power transformers share input current and power level, a higher turns ratio transformer can be replaced by two lower turns ratio transformers which allows a simple design and manufacturing of the transformers. Also it causes a lower AC resistance and leakage inductance due to it performances as a distributed magnetics.

Since two primary sides operate in-synchronism and in-phase utilizing the same control signals, a single branch can be analyzed as an example. Fig.2 shows basic waveforms for the primary-parallel isolated boost converter. Primary switches, S_1-S_4, are hard switched and operated in pairs, S_1-S_2 and S_3-S_4 respectively. Drive signals are 180 degree phase shifted. Switch transistor duty cycle, D, is above 50 percent to ensure switch overlap and thus a continuous current path for the inductor, L_1, current. Basic converter operation can be divided into four stages [21].

1) Stage 1 (T_1): All switches, S_1-S_4, are on and the inductor is charged. All rectifier diodes, D_1-D_4, are off and current in the transformer secondary winding is zero;

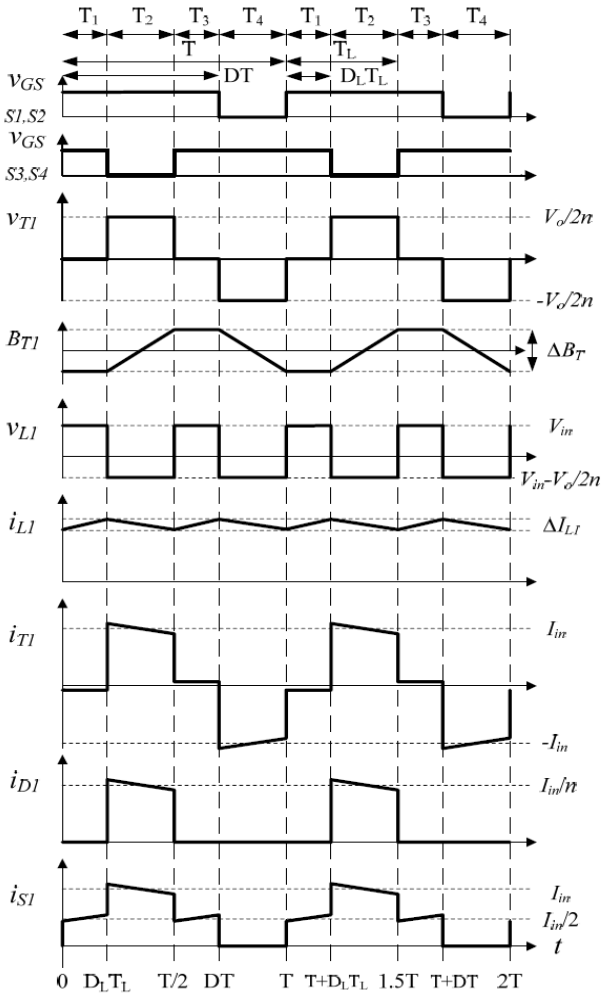

Fig. 2. Timing diagram and basic waveforms for isolated full-bridge boost converter.

2) Stage 2 (T_2): A first energy transfer period, T_2, starts when switches, S_3 and S_4, are turned off. Inductor current discharges flowing through primary switch, S_1, transformer, T_1, rectifier diodes, D_1 and D_2, and output capacitor, C, and returns to input through primary switch S_2;

3) Stage 3 (T_3): As the same as period T_1, when all switches are on, the inductor starts to be charged and i_{L1} increases linearly;

4) Stage 4 (T_4): Finally, a second energy transfer cycle, T_4, starts when switches, S_1 and S_2, are turned off. Inductor current discharges flowing through primary switch, S_3, transformer, T_1 (in opposite direction compared with first energy transfer period), rectifier diodes, D_3 and D_4, and output capacitor, C, and returns to input through primary switch S_4.

III. NEW PIM MODULE STRUCTURE

The conventional IM design currently uses soft-ferrite E-I or E-E core. In this work, a new PIM structure is proposed to integrate two independent transformers, T_1 and T_2, and two

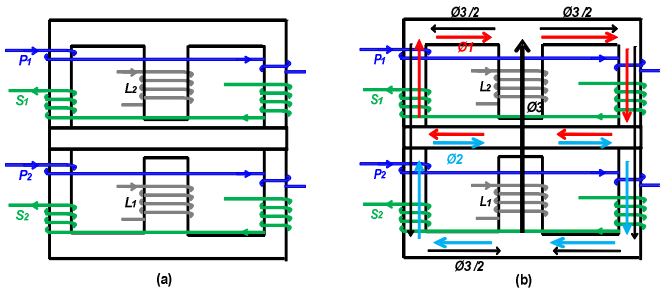

Fig. 3. (a) Proposed E-I-E integrated magnetic structure (b) instantaneous flux distribution.

input boost inductors, L_1 and L_2, with a combined E-I-E core geometry. The new PIM module is shown in Fig.3. The windings of each transformer are symmetrically distributed into the outer legs of E-cores. L_1 and L_2 are wound in the center legs of E-cores with certain air gaps. The middle I-core provides a low reluctance return path where complete flux cancellation can be achieved as shown in Fig.4. All the flux generated by the transformer windings circulate only through the outer legs of the E-cores. DC flux Φ_3 generated by the two input inductor windings goes through the two E-cores, and no DC flux exists in the shared I-core. As seen in Fig.3 or Fig.4, half of Φ_3 increases the total flux in the right side together with Φ_1 and Φ_2 and the other half of Φ_3 decreases it in the left side. Although the flux cancellations in this integration method will reduce the core loss, notice that a saturation problem may occur due to the flux overlapping in the half part of the PIM module which limits the nominal power of the converter.

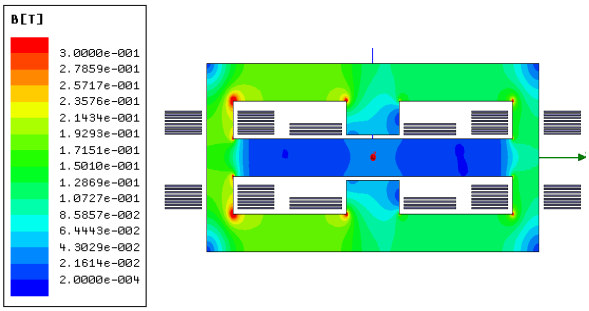

Fig. 4. Flux distribution in the core for the proposed PIM structure.

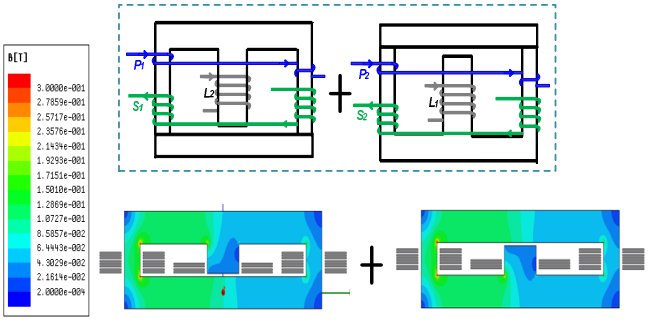

Fig. 5. Flux distribution in the core for a separate case.

In term of this new geometry, many advantages can be concluded as follows,

(1) Air gaps located in the center legs cause a lower fringing effect as well as EMI problem [2], [9]. Mechanically stabilization is also counted as an advantage for the location of air gaps.

(2) Magnetizing inductances of the transformers will not be decreased even if the air gap exists in the core. This is because the flux Φ_1 and Φ_2 circulate through the outer legs of the E-cores rather than the center legs with air gaps. Furthermore, integrated transformers in this geometry have higher magnetizing inductance compared to the separated case which can be mathematically proved in section IV.

(3) The total core loss in the PIM module is lower than that in the discrete magnetics. This is because many flux cancellation occurs in the core geometry.

(4) Less number of cores can be used, causing a low cost for the converter.

(5) The integrated approach provides a low footprint for the converter, which increases the power density required by the space restriction in automotive and integrated application.

(6) Flexibility. The integrated approach can be extended into many other topologies.

IV. Magnetics Design Consideration

Fig.6 shows an equivalent magnetic reluctance model of the PIM module where R_1 is the reluctance of each outer leg of E-core, R_2 is half reluctance of I-core and R_C represents the reluctance of the center leg of E-core. R_C is much bigger than

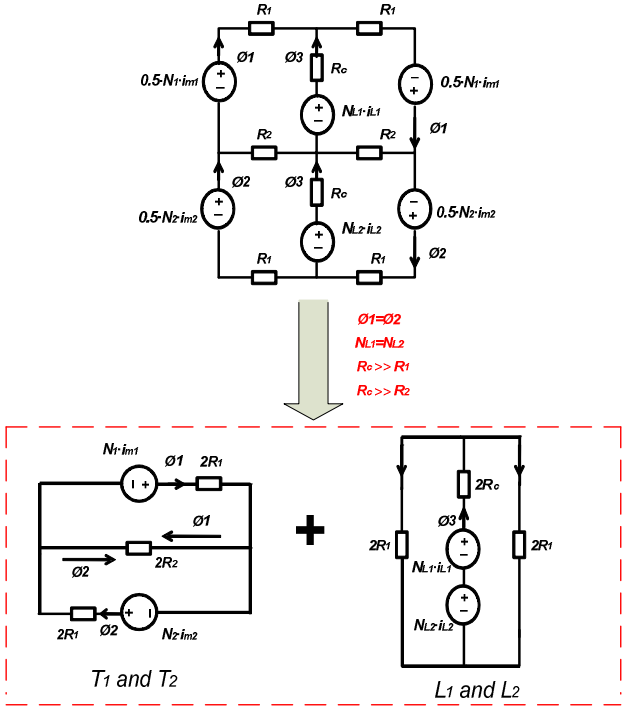

Fig. 6. Magnetic reluctance model of the new PIM structure.

R_1 and R_2 because of the air gaps of the center legs. Since the transformers and the inductors have not been affected each other (uncoupled), the equivalent magnetic model can be divided into two parts as shown in the bottom of Fig.6. The left part represents the magnetic model associated with T_1 and T_2. The flux Φ_1 and Φ_2 never go through the center legs. The flux Φ_1 and Φ_2 in the shared I-core will be completely cancelled. In fact, the flux Φ_1 is identical to the flux Φ_2 due to two transformers operate in-phase currents utilizing the same control signals. The right part represents the magnetic model of the two inductors, L_1 and L_2. The flux in the outer legs are different this is the fact that the half of flux Φ_3 blocks Φ_1 and Φ_2 and the other half promotes them.

With assumption that leakage flux through the air is negligible, (1) ~ (3) can be obtained according the magnetic model,

$$N_1 \cdot i_{m1} = \phi_1 \cdot 2R_1 + (\phi_1 - \phi_2) \cdot 2R_2 \quad (1)$$

$$N_2 \cdot i_{m2} = \phi_2 \cdot 2R_1 + (\phi_2 - \phi_1) \cdot 2R_2 \quad (2)$$

$$2 \cdot N_L \cdot i_L = \phi_3 \cdot 2R_c + 0.5 \cdot \phi_3 \cdot 2R_1 \quad (3)$$

The rate of change on Φ_1 and Φ_2 are the same over an entire period. Based on Faraday's law, magnetizing inductances can be obtained,

$$L_{m1} = \frac{N_1^2}{2R_1} \quad ; \quad L_{m2} = \frac{N_2^2}{2R_1} \quad ; \quad L_1 = L_2 = \frac{2 \cdot N_L^2}{2R_c + R_1}$$

Regarding to the separate case (non-integrated transformers), the magnetizing inductance is equal to, $L_m = N^2 / (2R_1+2R_2)$. As can be seen, such integrated transformers have higher magnetizing inductance compared to the separated case. This is because of the fact that the flux cancellation occurs in the shared I-core effectively reducing the length and reluctance of the transformer flux path.

According to Faraday's law and Ampere's law, the peak flux densities of each magnetic component in the PIM module can be derived,

$$B_{pk\_T} = \frac{V_{out} \cdot (1-D)}{4 \cdot n \cdot f \cdot N \cdot A_e} \quad (4)$$

$$B_{pk\_L} = \frac{\mu_0 \cdot N_L \cdot I_{pk}}{l_g} \quad (5)$$

where D is switching duty cycle, n is turns ratio of both transformers, f is switching frequency and A_e is cross-section of the outer leg of the core. l_g is length of the air gap in each center leg. In order to avoid flux saturation in the PIM module, the following equations are required,

$$B_{pk\_T} + B_{pk\_L} = \frac{V_{out} \cdot (1-D)}{4 \cdot n \cdot f \cdot N_1 \cdot A_e} + \frac{\mu_0 \cdot N_L \cdot I_{pk}}{l_g} \le B_{sat} \quad (6)$$

The power capability of the module can be increased by minimizing the peak flux density of transformer, which can be implemented by increasing either the frequency or the number of turns. But both methods may not conducive to the power efficiency.

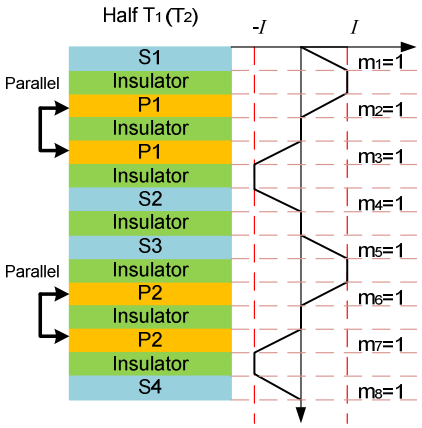

Fig. 7. Winding arrangement and MMF distribution for half winding of the transformer symmetrically wound in one of the outer legs.

Winding losses in transformers increase dramatically with high frequency due to eddy current effects. Eddy current losses, including skin effect and proximity effect losses seriously impair the performance of transformers in high-frequency power conversion applications. Both the skin effect and the proximity effect cause the current density to be non-uniformly distributed in the cross-section of the conductor, and thus cause a higher winding resistance at higher frequency. The proximity effect loss, in a multilayer winding, may strongly dominate over the skin effect loss depending on winding arrangement. Interleaving transformer windings can reduce the proximity loss significantly when the primary and secondary currents are in-phase. Fig.7 shows the winding arrangements and magneto motive force (MMF) distributions

TABLE I. Magnetics Design Results

Parameters	Values
Number of turns in primary (N_1=N_2)	4
Turns ratio of each transformer	1:2
Number of turns for the inductors (N_{L1}=N_{L2})	4
Each air gap length (l_g)	0.5mm
Core type	EILP 64
Core material	Ferrite N87
Copper thickness for each layer of PCB winding	4 OZ (140um)
Switching frequency	50 kHz
AC resistance referring to the secondary side	231.5 mΩ
Leakage inductance referring to the secondary side	906.6 nH
Magnetizing inductance referring to the secondary side	638 uH
Inductance of input inductor (L_1)	21.1 uH
Inductance of input inductor (L_2)	20.4 uH
AC resistance of input inductor L_1 (100-kHz)	60.8 mΩ
AC resistance of input inductor L_2 (100-kHz)	64.9 mΩ

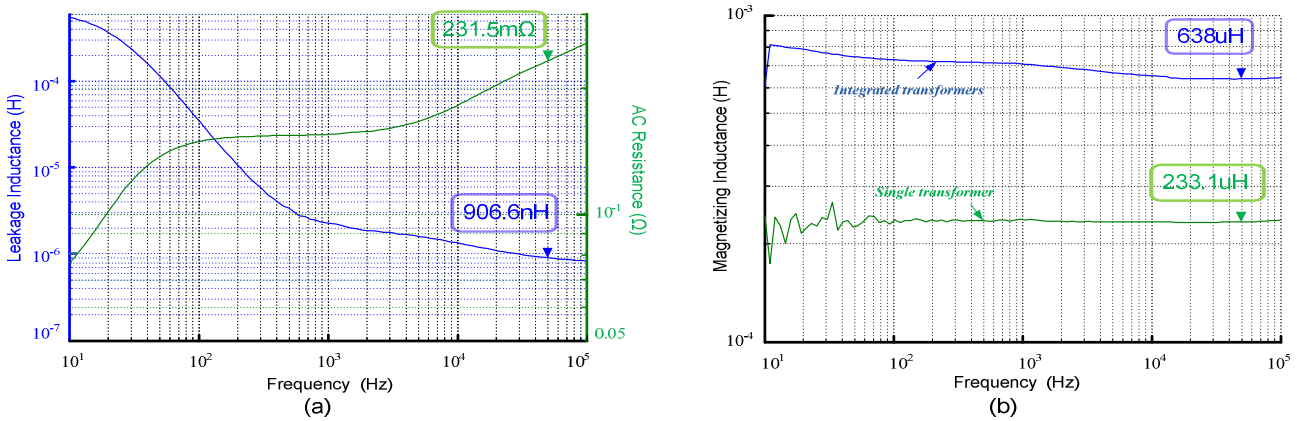

Fig. 8. Measurement results for integrated transformer by impedance analyzer. (a) ac resistance and leakage inductance referring to the secondary side. (b) magnetizing inductance referring to the secondary side.

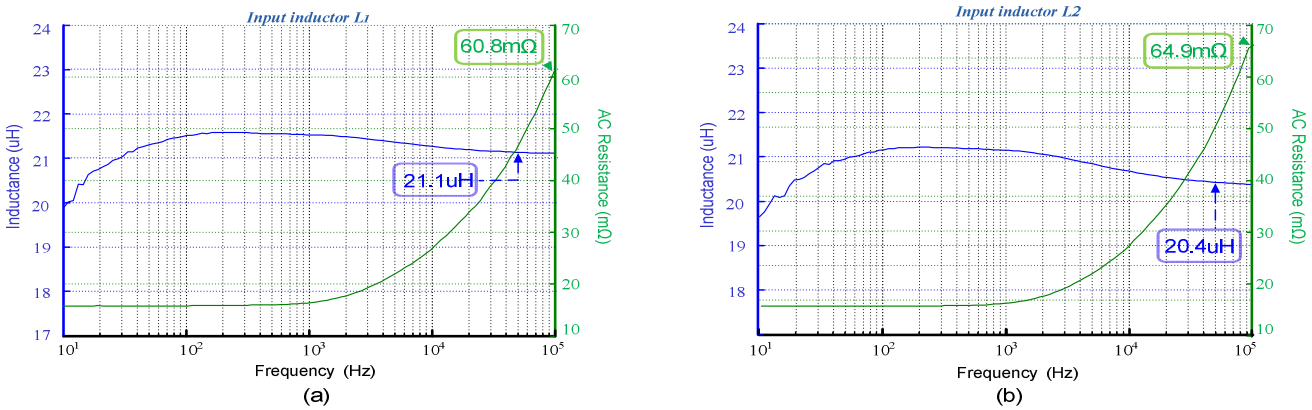

Fig. 9. Measurement results. (a) ac resistance and inductance for L_1. (b) ac resistance and inductance for L_2.

alone the vertical direction for half winding of transformer T_1 or T_2 symmetrically wound in one of the outer legs. The MMF ratio m [23], [24] in each layer is equal to 1 which contributes a lower AC resistance.

Not only AC resistance can be reduced, but also leakage inductance can be significantly decreased by interleaving winding [22]. Notice that interwinding capacitance in this kind of interleaving arrangement is much better than full interleaving arrangement without sacrificing any other behaviors such as leakage inductance and AC resistance because of fewer intersections between the primary and the secondary, contributing a relative lower EMI problem [24].

V. Experimental Results

A 1-kW prototype converter has been built to verify the new integrated magnetics design approach. Input voltage is between 20-40 V and output voltage is 170-230 V. Primary switches are IPA028N08N3, 80-V, 2.8-mΩ power MOSFETs from Infineon. Output rectification is handled by V30200C Schottky diodes with 0.65-V forward voltage drop. The designed specification and magnetic results of the PIM module are shown in Table I. The PIM module uses EILP-64 cores with N87 core material. Transformer turns ratio is 1:2 (n=2). Air gaps with both 0.5-mm lengths are used for the storage inductors L_1 and L_2. 4-OZ copper thickness is used for PCB windings. Interleaving technique shown in Fig.7 is used to decrease AC resistances and leakage inductances.

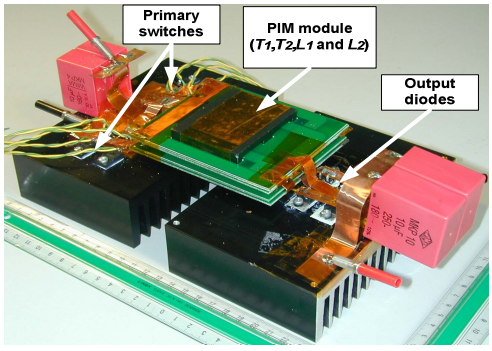

Fig. 10. Experimental prototype of the primary-parallel isolated boost converter employing the PIM module.

The measurement results for the two integrated transformers in the PIM module are shown in Fig.8, obtained by PSM1735, impedance analyzer. The stray parameters of the circuit are included in the measurement results as well. All results are referred to the secondary side. Assuming that T_1 and T_2 have exact same parameters, 113-nH leakage inductance and 29-mΩ ac resistance referred to the primary sides of each transformer can be derived. The measurement results for the two integrated inductors are shown in Fig.9. Switching frequency is 50-kHz with inductor current ripple of

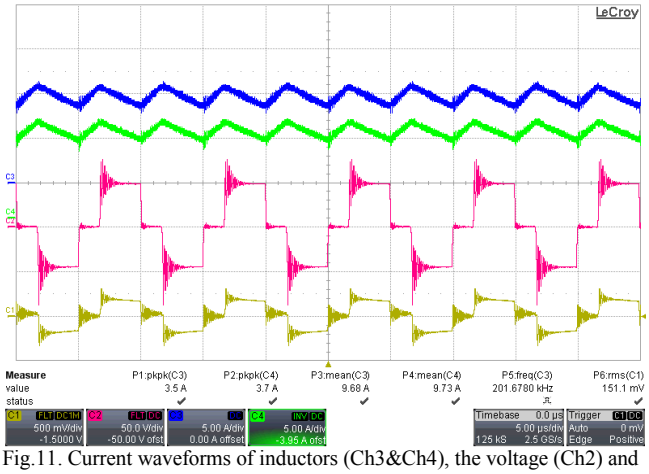

Fig.11. Current waveforms of inductors (Ch3&Ch4), the voltage (Ch2) and the current (Ch1) of T_1.

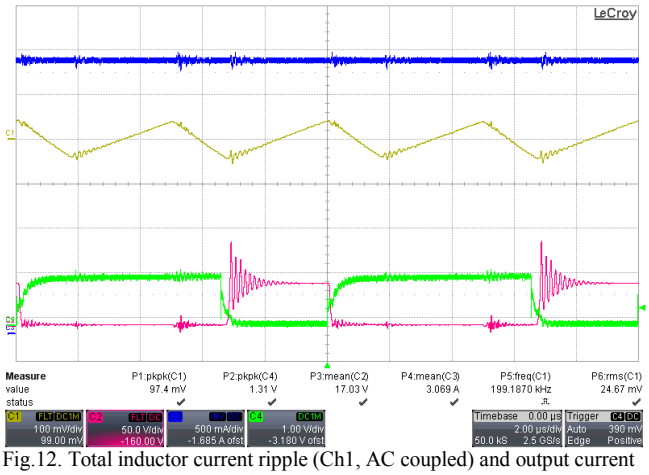

Fig.12. Total inductor current ripple (Ch1, AC coupled) and output current (Ch3), V_{DS} (Ch2) and V_{GS} (Ch4) of S_1.

100-kHz. The ac resistances have a slight difference which is mainly due to different distances away to the air gap of the center leg from the windings, causing different fringing effects.

IRS2110 high and low side gate drivers are used in the gate driver circuit together with ISO722C capacitive digital isolators for control signal protection. The control signals are produced by TMS28027 DSP. Fig.10 shows the implemented prototype with all the switches mounted on a heat sink. Output is filtered by two 10-uF capacitors placed very close to the rectifiers for minimizing the ac loop. When the converter operates at 100-kHz, 30-V input, 180-V output and 600-W output power, the current waveforms of inductors (Ch3&Ch4), the voltage (Ch2) and the current (Ch1) of transformer T_1 are presented in Fig.11. Observe that the two currents are identical. Removing oscilloscope offset, causes current traces to fully coincide. Also the total inductor current ripple (Ch1, AC coupled) and output current (Ch3), V_{DS} (Ch2) and V_{GS} (Ch4) of S_1 are shown in Fig.12 respectively.

High stability (< 10 ppm) 0.1 % shunt resistors are used for high precision of the efficiency measurements. Agilent 34410A high precision multimeters are used for all measurements. Current sense signals are shielded and fitted with common mode filters. Efficiency curves of the converter employing the PIM module when the output voltage is 180-V are shown in Fig.13. As can be seen, the converter has higher efficiency in the light load when the input voltage is low. This is because of the fact that the core loss mainly dominates over the total power loss in the light load. For a low input voltage, a higher duty cycle D is required for achieving a constant output voltage due to voltages ratio is $V_o/V_{in}=n/(1-D)$. According to Faraday's law, the peak to peak flux density of transformer can be expressed by,

$$\Delta B_T = \frac{V_0 \cdot (1 - D)}{2 n \cdot f \cdot N \cdot A_e} \tag{7}$$

Equation (8) can be expressed in terms of the input voltage, V_{in}, by substitution of voltages ratio.

$$\Delta B_T = \frac{V_{in}}{2 \cdot f \cdot N \cdot A_e} \tag{8}$$

Therefore, a lower input voltage causes a lower peak to peak flux density of transformer which contributes a lower core loss. With increasing the switching frequency, the differential of the peak to peak flux density ΔB_T in different input voltages becomes small. The efficiencies in the light load therefore become to be close. Oppositely, winding loss strongly dominates over the total power loss in the heavy load. Higher input voltage has higher efficiency in this case. Maximum efficiency of 96% has been observed with 40-V

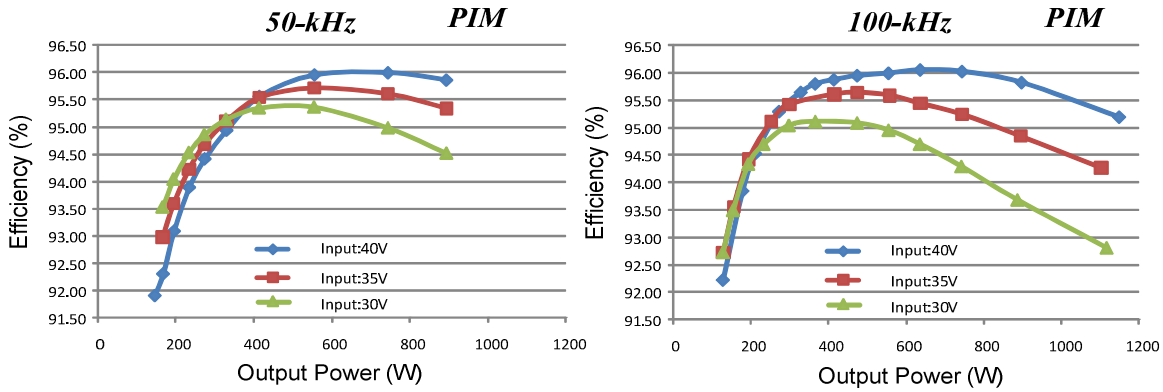

Fig. 13. Efficiency curves of the converter with PIM module when output voltage is 180-V.

input voltage, 180-V output voltage and 800-W output power. Worst case efficiency, at minimum input voltage 30-V and maximum load, is 94.5 %.

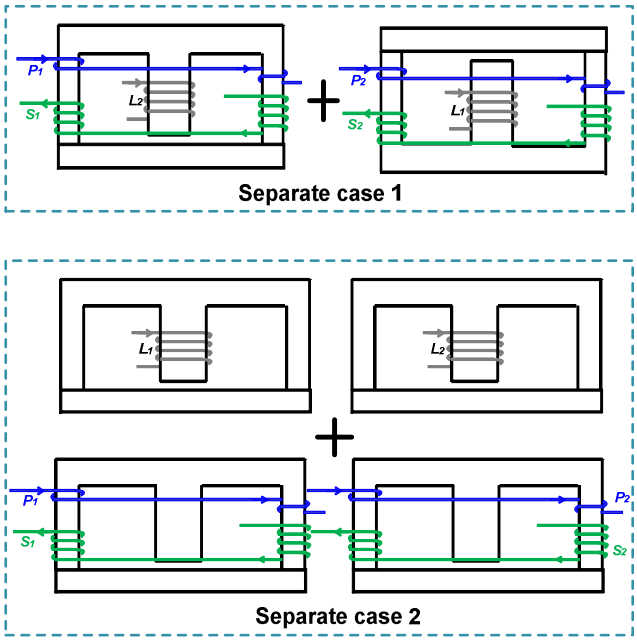

Fig.14. Separate cases for an experimental comparison.

In order to illuminate the PIM module has a higher efficiency, experimental comparisons between the PIM module and two separate cases has been done. Keeping the same PCB windings, the case-1 has two separate E-I cores by adding a single I-core. A single inductor and a single transformer are still integrated into the E-I core. The case-2 completely separates the four discrete magnetic components, L_1, L_2, T_1 *and* T_2, and the windings of transformer still keep the same arrangements with those of the PIM module in order to get a relative fair comparison. Obviously, the PIM module has the smallest footprint and fewest numbers of components which causes a higher power density and lower cost. Furthermore, higher efficiencies can be achieved for the PIM module in both full range loads and full range input voltages. It can be seen from Fig.15 that the separate case-2 has a higher efficiency than the separate case-1 when the converter is working under 50-kHz and 30-V input voltage. This is because the core loss in the case-1 is very sensitive to the peak to peak flux generated by the inductors, ΔB_L. Since the flux Φ_1 of transformer has been inside the core already, the core loss will be highly increased by adding a few peak to peak flux ΔB_L. By increasing either the switching frequency or the input voltage, the peak to peak flux ΔB_L becomes small, and then the two efficiencies will be close. There is an approximate 1.3% improvement of efficiency between the PIM module and the case-2 when the converter works at 50

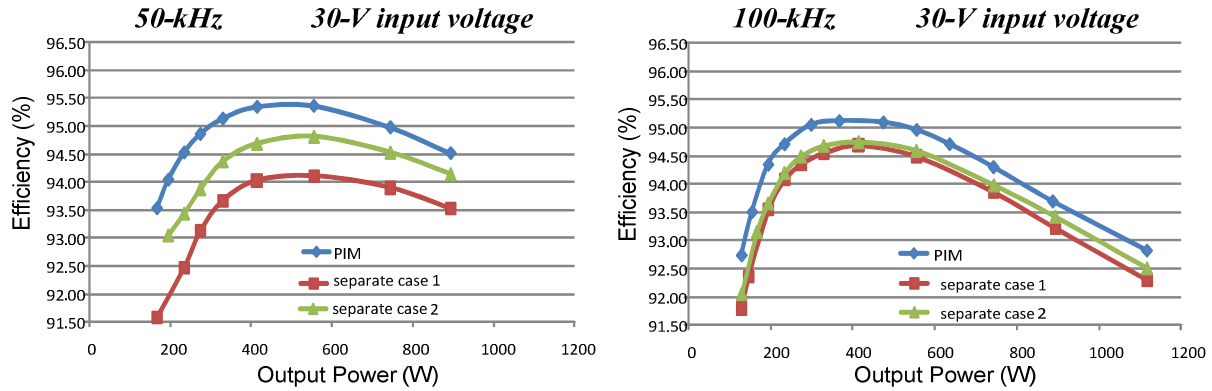

Fig. 15. Efficiency comparisons between PIM and two separate cases at 30-V input voltage and 180-V output voltage

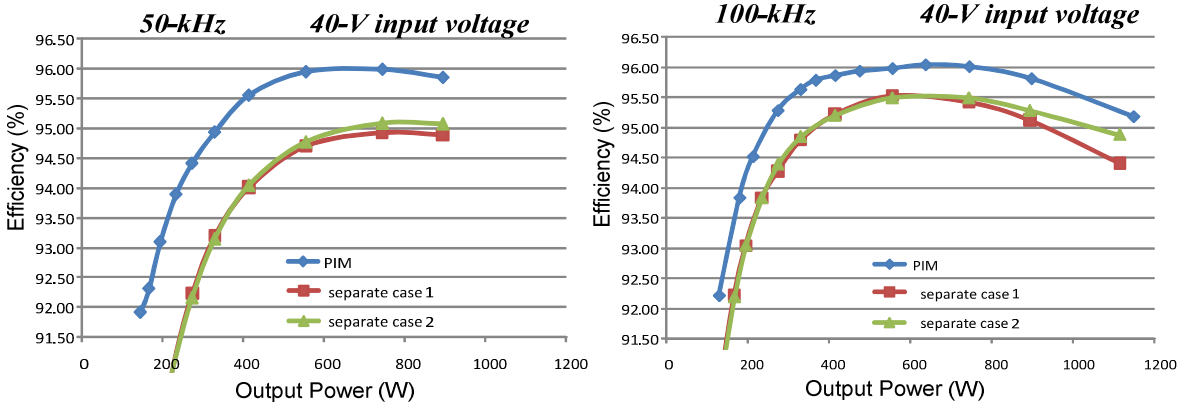

Fig. 16. Efficiency comparisons between PIM and two separate cases at 40-V input voltage and 180-V output voltage

kHz and 600-W output power. This improvement will be decreased to approximate 0.5% if the switching frequency is up to 100-kHz due to the rate of the core loss dominates over the total loss becomes small.

VI. Conclusion

This work presents a new geometry E-I-E magnetics integration method in order to integrate two individual transformers and two boost input inductors for primary-parallel isolated boost converter. The new PIM design approach provides a low footprint, high power density, low cost and higher efficiency alternative to the discrete design. Test resulting from a 1-kW experimental prototype verifies that converter employing the PIM module is fully functional and electromagnetically equivalent. An efficiency of 96% can be achieved during the nominal operating conditions. Experimental comparisons between the PIM module and two separate cases demonstrate that lower footprint and higher efficiency for the PIM module.

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Appendix A8

[A8] Z. Ouyang, **G. Sen**, O. C. Thomsen, M. A. E. Andersen, "Analysis and design of fully integrated planar magnetics for primary-parallel isolated boost converter," IEEE Transactions on Industrial Electroics, 2012 (**In press**, digital object identifier: 10.1109/TIE.2012.2186777).

Analysis and Design of Fully Integrated Planar Magnetics for Primary-Parallel Isolated Boost Converter

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***Abstract*—A high efficient planar integrated magnetics (PIM) design approach for primary-parallel isolated boost converters is presented. All magnetic components in the converter including two input inductors and two transformers with primary-parallel and secondary-series windings are integrated into an E-I-E core geometry, reducing the total ferrite volume and core loss. The transformer windings are symmetrically distributed into the outer legs of E-cores and the inductor windings are wound on the center legs of E-cores with air gaps. Therefore, the inductor and the transformer can be operated independently. Due to the low reluctance path provided by the shared I-core, the two input inductors can be integrated independently, and also the two transformers can be partially coupled each other. Detailed characteristics of the integrated structure have been studied in this paper. AC losses in the windings and the leakage inductance of the transformer are kept low by interleaving the primary and secondary turns of the transformers substantially. Because of the combination of inductors and transformers, maximum output power capability of the fully integrated module needs to be investigated. Winding loss, core loss and switching loss of MOSFETs are analyzed in-depth in this work as well. To verify the validity of the design approach, a 2-kW prototype converter with two primary power stages is implemented for a fuel cell fed traction applications with 20-50 V input and 400-V output. An efficiency of 95.9% can be achieved during 1.5-kW nominal operating conditions. Experimental comparisons between the PIM module and three separated cases have illustrated the PIM module has advantages of lower footprint and higher efficiencies.**

***Index Terms*— Core loss, dc-dc converter, fuel cell, inductor, isolated boost, planar integrated magnetics (PIM), transformer and winding loss.**

I. Introduction

DISTRIBUTED generation systems, back-up systems or traction systems based on fuel cells or batteries, requires high-power high-gain dc-dc converters to boost the low source voltage (20-50 V) to a higher dc-link voltage (350-400 V). For safety or EMC reasons, transformer isolation is often required or preferred. As power levels increase, input currents quickly reach levels where paralleling of primary switches become necessary. Since transistors are often operated close to their maximum drain current rating, direct paralleling of MOSFETs may require screening and parameter matching of on-resistance, gain and/or threshold voltages. Slowing switching speed by increasing gate impedance or addition of source inductance may also be required. A new, simple and low cost method to extend power level in isolated boost converters by paralleling of critical high-ac-current circuit parts is presented in [1]. It is found that the ac-current loop from the primary switches to the transformer primary windings is a particularly critical area with respect to scaling of power level. This requires extremely low leakage inductance of transformers and stray inductance of the circuit layout in order to achieve high efficiency. With traditional magnetics components, this extreme requirements result a high cost in magnetics components and an impossibility of mass production, although 98.2% peak efficiency can be achieved in this converter. Moreover, the size of magnetics components also limits its application in practice.

In order to satisfy the requirements of modern power electronics application, magnetics integration with planar core has proven to be an effective means of reducing the converter size and cost, while increasing the converter efficiency. Planar magnetics have unique advantages in terms of increased power density, better cooling capability, modularity and manufacturing simplicity as well as easy implementation of interleaved windings, which make them attractive for high current dc-dc power converter applications [2]-[13]. In recent years, most efforts in integrated magnetics (IM) focus on the current-doubler rectifier due to its suitability for low-output-voltage and high-output-current applications. Unlike conventional magnetic integration focusing only on core integration, both core and winding integration can be realized in the current-doubler rectifier design, causing lower conduction loss and core loss. As a result, lower overall cost, size as well as higher efficiency can be obtained by the IM design for the current-doubler circuit [2]–[6] and the dual-inductor isolated boost converter as well [14]. A 1-kW module with 300~400-V input voltage and 48-V output voltage asymmetrical half-bridge PWM converter employing an integrated L–L–C–T module is constructed in [7]. Detailed suggestions are given on how a generic, integrated LCT component could be used to implement various resonant converter topologies by merely reconfiguring the external terminals of the integrated components [8]-[9]. An integrated transformer consisted of four step-down transformers wound on a single magnetic core for an interleaved four-phase forward converter has been proposed in [15]. Coupled inductors greatly reduce the steady-state inductor current ripples without sacrificing the transient response as shown in [16]-[19]. A full procedure to generate 2D Finite Element Analysis (FEA) based model for integrated magnetics is presented in [20].

The converter in [1] is a typical application of distributed magnetics. Distributed magnetics functionally split a large magnetic element into small magnetic element which is an efficient way to reduce ac resistance and leakage inductance compared to a large single magnetic component [21]. Over 40% of the effective winding resistance and 20% leakage inductance reduction can be achieved by matrix transformers [22], making it very attractive for high current applications. However, increased numbers of components in the distributed magnetics increases the size of the power converters and reduces the power efficiency in the light load due to higher core loss. Therefore, integration of

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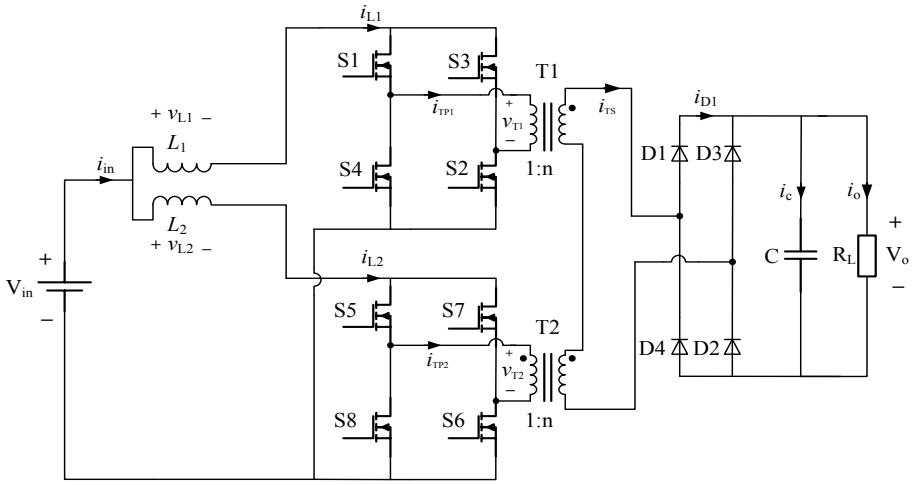

Fig. 1. Primary-parallel isolated boost converter.

distributed magnetics becomes promising. In this paper, a new approach to integrate the distributed magnetics components for the primary-parallel isolated boost converter is presented. All magnetic components in the converter including the two input inductors and two transformers with primary-parallel and secondary-series connected windings are integrated into an E-I-E core geometry, reducing the total ferrite volume and core loss. The transformer windings are symmetrically distributed into the outer legs of E-cores and the inductor windings are wound on the center legs of E-cores with air gaps. Detail characteristics of the integrated structure are presented in Section III. Due to the integration of inductors and transformers, maximum output power capability of the integrated module has to be considered to avoid flux saturation in the core. Core loss estimation for the PIM structure has been investigated in-depth and an effect of core loss under dc bias operation has been considered as well. AC losses in the windings and leakage inductance of the transformers are kept low by interleaving the primary and secondary turns of the transformers. A detailed power loss analysis is given in section V. To verify the validity of the design approach, a 2-kW prototype converter with two primary power stages is implemented for fuel cell fed traction applications with 20~50-V input and 400-V output. An efficiency of 95.9% can be achieved during 1.5-kW nominal operating conditions. Experimental comparisons are presented in section VI show the advantages of low profile and high efficiency for the PIM module. In addition, the proposed PIM approach can solve the start-up problem of the boost converter without adding external Flyback winding [23].

II. Primary-Parallel Isolated Boost Converter

Boost derived topologies are preferred in fuel cell applications due to their low input current ripple [24]. Fig.1 shows a primary-parallel isolated boost derived topology suitable for handling high input currents for fuel cell applications. Series connection of transformer secondary windings ensures current sharing during energy transfer cycle when power is transferred to output. In this topology, primary power stages share the same control signals with same phase switching sequence for the corresponding switches which allows a simpler control. Output rectification unit as well as input and output filters are common to both of the primary stages. The paralleling method splits the critical primary high-ac-current-loop into two smaller loops. Each of the smaller

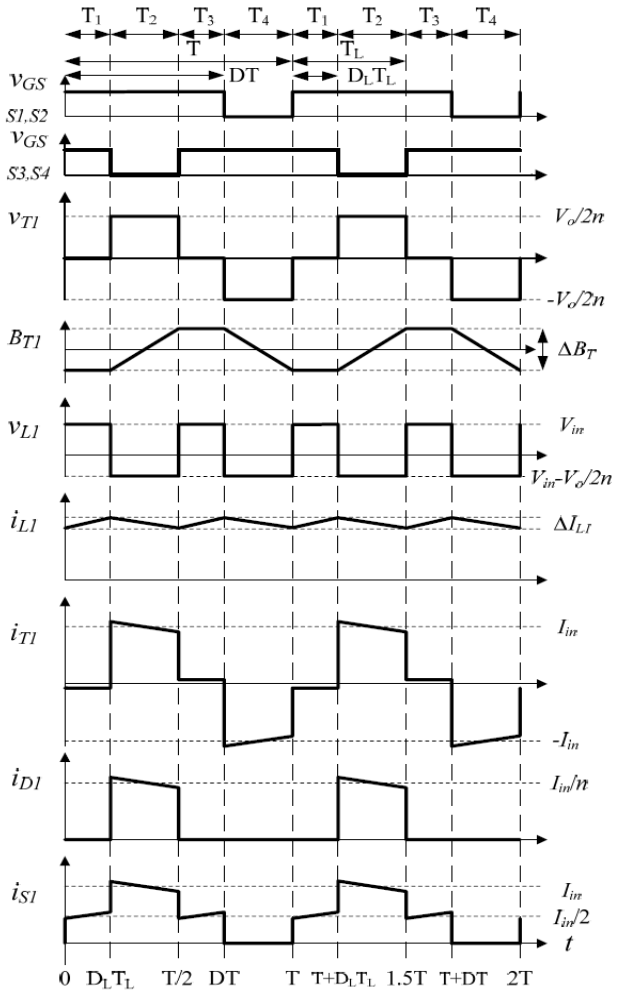

Fig. 2. Timing diagram and basic waveforms for primary-parallel isolated boost converter.

loops only needs to switch half of the input current thereby achieving much faster current switching and thus higher conversion efficiency. Since the two transformers T_1 and T_2 share input current and power level, a higher turns ratio transformer in the conventional full-bridge isolated boost converter can be replaced by two individual transformers with lower turns ratio which allows a simpler design and manufacturing of the transformers.

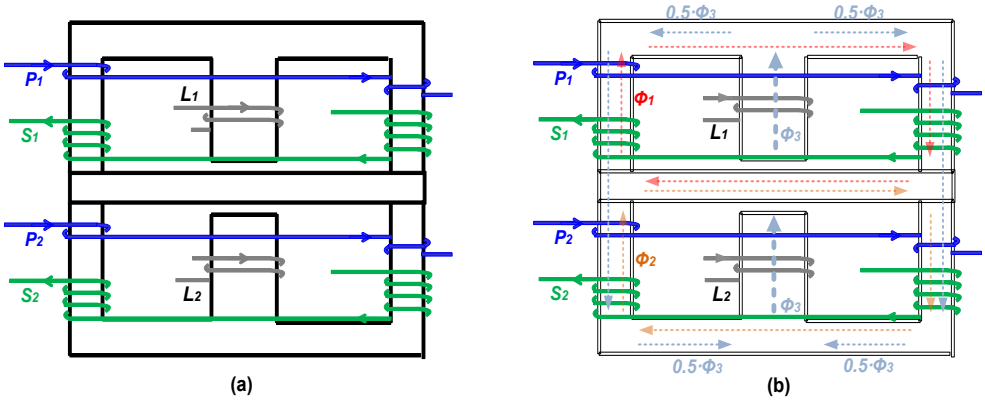

Fig. 3. Proposed E-I-E integrated magnetic structure (a) and its instantaneous flux distribution (b).

Since the two primary stages operate synchronously utilizing the same control signals, a single stage is analyzed as follows. Fig.2 shows basic waveforms of the primary-parallel isolated boost converter. Primary switches, S_1~S_4, are hard switched and operated in pairs, S_1~S_2 and S_3~S_4 respectively. Driving signals are 180˚ phase shifted. Switch transistor duty cycle, D, is above 50% to ensure switch overlap and thus a continuous current path for the boost inductor current. The basic converter operation can be divided into four stages [24].

1) Stage 1 (T_1): All switches, S_1~S_4, are on and the inductor is charged. All rectifier diodes, D_1~D_4, are off and current in the transformer secondary winding is zero;

2) Stage 2 (T_2): The first energy transfer period, T_2, starts when switches, S_3 and S_4, are turned off. Inductor energy discharges with its current flowing through primary switch, S_1~S_2, and transformer, T_1 primary. The current in the secondary side flows through the rectifier diodes, D_1~D_2, and the output capacitor, C.

3) Stage 3 (T_3): Works the same as *stage 1*, all switches are turned on, the inductor is charged and the inductor current, i_{L1}, increases linearly;

4) Stage 4 (T_4): The second energy transfer cycle, T_4, starts when switches, S_1 and S_2, are turned off. Inductor energy discharges with its current flowing through primary switches, S_3~S_4, transformer, T_1 primary. The current in the secondary side flows through the rectifier diodes, D_3 and D_4, and the output capacitor, C.

III. Modeling of Integrated Magnetics

Two separated transformers and one boost inductor are integrated into an E-I-E core geometry for hybrid dc-dc converter in [25]. In this study, an additional inductor is added into a combined E-I-E core geometry where two independent transformers, T_1 and T_2, and two boost inductors, L_1 and L_2, are integrated. Fig.3 shows the proposed integrated magnetics structure. The windings of each transformer are symmetrically distributed into the outer legs of the two E-cores. L_1 and L_2 are wound on the center legs of E-cores with air gaps. The middle I-core provides a low reluctance return path where a complete flux cancellation can be achieved since the two transformers, T_1 and T_2, operate with in-phase currents utilizing the same control signals. In fact, the shared I-core could be removed where E-I-E geometry becomes E-E geometry since zero flux is in the shared I-core. However, the two inductors, L_1 and L_2 will be fully direct coupled if the shared I-core is removed. This results in a huge spike of inductor current at commutation point if there is any small mismatch in two primary stages [26]. Accordingly, the effect of the shared I-core is to decouple the two inductors. The flux generated by the transformer windings circulate only through the outer legs of the E-cores, which does not affect the inductor's behavior. As shown in Fig.3 (b), flux Φ_3 (include dc component) generated by the two input inductor windings goes through the two E-cores, and no dc flux exists in the shared I-core due to the cancellation. As seen in Fig.3, at a certain time period, half of Φ_3 increases the total flux in the right leg together with Φ_1 and Φ_2 and the other half of Φ_3 decreases it in the left side. A reverse situation will occur during the next time period. As a result, Φ_3 will not affect transformer's behavior. Hereby, the transformers and the inductors are not coupled electro-magnetically although the windings are wound in the same core. The flux waveforms in each leg are presented in Fig.9. The proposed structure features an uncoupled technique for all magnetic components in the primary-parallel converter, and there may not have other possible configuration unless using the customer design core geometries instead of the standard core geometries.

Fig.4 shows an equivalent magnetic reluctance model of the PIM module where R_1 is the reluctance of the outer leg of E-core, R_2 is the reluctance of I-core and R_C represents the reluctance of the center leg of E-core. R_C is much bigger than R_1 and R_2 due to the air gaps in the center legs. Since the transformers and the inductors are not coupled electromagnetically, the equivalent magnetic model can be divided into two parts as shown in the bottom of Fig.4. The left figure represents the magnetic model associated with T_1 and T_2. The flux Φ_1 and Φ_2 does not flow in the center legs of the E-core. The flux Φ_1 is identical to the flux Φ_2 due to two transformers operate with in-phase currents utilizing the same control signals. Therefore, the flux Φ_1 and Φ_2 in the shared I-core are fully cancelled. The right figure represents the magnetic model of the two inductors, L_1 and L_2.

With the assumption that the leakage flux through the air and the fringing effect are negligible, equations (1) ~ (3) can be derived according to the magnetic model,

$$N_1 \cdot i_{m1} = \Phi_1 \cdot (2R_1 + R_2) + (\Phi_1 - \Phi_2) \cdot R_2 \tag{1}$$

$$N_2 \cdot i_{m2} = \Phi_2 \cdot (2R_1 + R_2) + (\Phi_2 - \Phi_1) \cdot R_2 \tag{2}$$

$$2 \cdot N_L \cdot i_L = 2 \cdot \Phi_3 \cdot R_c + 0.5 \cdot \Phi_3 \cdot (2R_1 + R_2) \tag{3}$$

where N_1 and N_2 are the number of primary turns for the transformers T_1 and T_2 respectively. N_L is the number of turns for

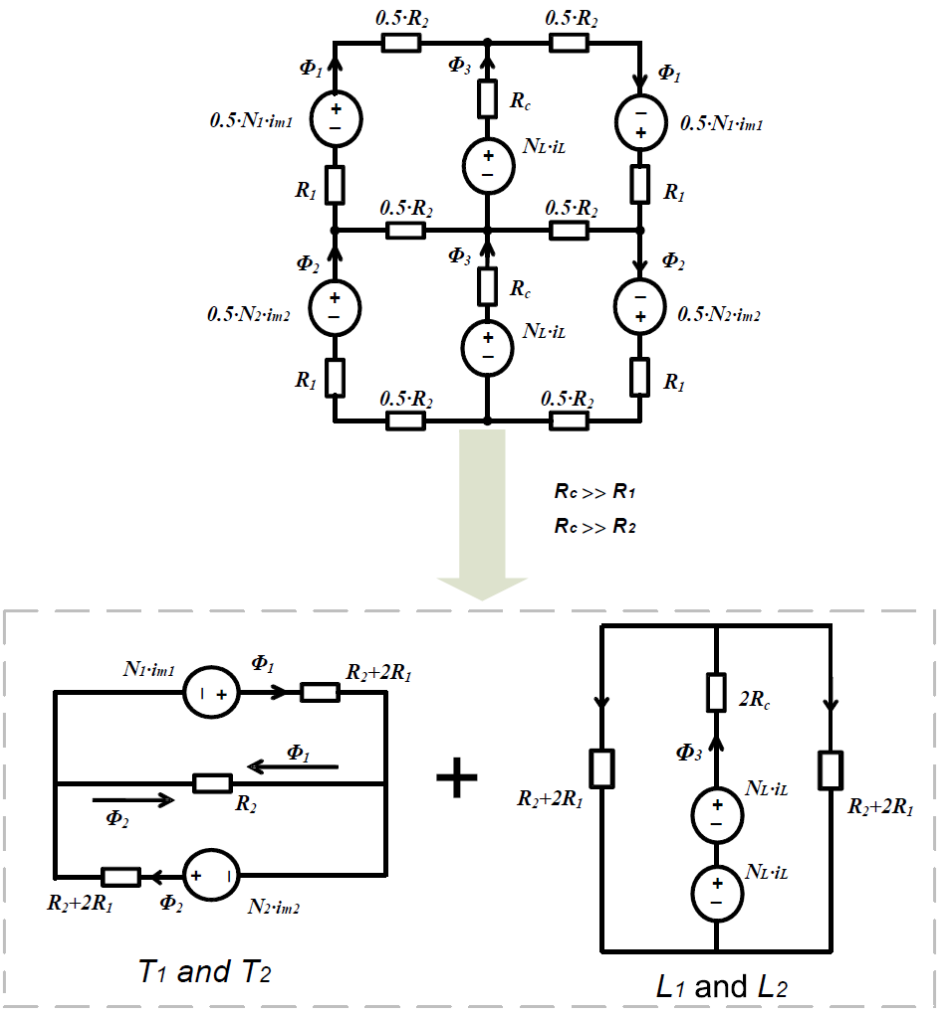

Fig. 4. Magnetic reluctance model of the PIM structure.

the inductors L_1 or L_2. The rate of change on Φ_1 and Φ_2 are the same over the entire period. Based on the Faraday's law, magnetizing inductances can be obtained,

$$L_{m1} = \frac{N_1^2}{2R_1 + R_2} \tag{4}$$

$$L_{m2} = \frac{N_2^2}{2R_1 + R_2} \tag{5}$$

$$L_1 = L_2 = \frac{2 \cdot N_L^2}{2 \cdot R_c + R_1 + 0.5 \cdot R_2} \tag{6}$$

For a single separated transformer with the same winding arrangement at the outer leg, the magnetizing inductance is equal to, $L_m = N^2 / 2(R_1+R_2)$, where N is the number of primary turns for the single transformer. It is important to note that the integrated transformers have higher magnetizing inductances than the single case when both T_1 and T_2 have same current excitation. This is due to the fact that the mutual inductance between the two transformers T_1 and T_2 increases the magnetizing inductance. The coupling effect between T_1 and T_2 is shown in appendix.

IV. Magnetics Design Consideration

The advantages of this structure are highlighted in [27]. Table-I has shown the integrated module has advantages in the cost, the efficiency, the size and the manufacturability at expense of the design process. Another drawback of the PIM module is to limit the maximum output power capability due to the overlapped flux. According to Faraday's law and Ampere's law, the peak flux densities of each magnetic component in the PIM module can be derived,

$$\hat{B}_T = \frac{V_{out} \cdot (1 - D)}{4 \cdot n \cdot f \cdot N \cdot A_e} \tag{7}$$

$$\hat{B}_L = \frac{\mu_0 \cdot N_L \cdot I_{pk}}{l_g} \tag{8}$$

$$\hat{B}_{Lac} = \frac{\mu_0 \cdot N_L \cdot \Delta I}{2 \cdot l_g} \tag{9}$$

where the peak current for the inductor is,

$$I_{pk} = I_{dc} + \frac{\Delta i}{2} = \frac{P_0}{\eta \cdot V_{in}} + \frac{V_{in} \cdot (D - 0.5) \cdot l_g}{2 \cdot f \cdot \mu_0 \cdot N_L^2 \cdot A_e} \tag{10}$$

TABLE I

COMPARISONS BETWEEN INTEGRATED AND CONVENTIONAL MAGNETIC COMPONENTS

	Integration	Convention
Cost	*Low*	*High*
Efficiency	*High*	*Low*
Size	*Small*	*Large*
Manufacturability	*Simple*	*Complex*
Design process	*Complex*	*Simple*

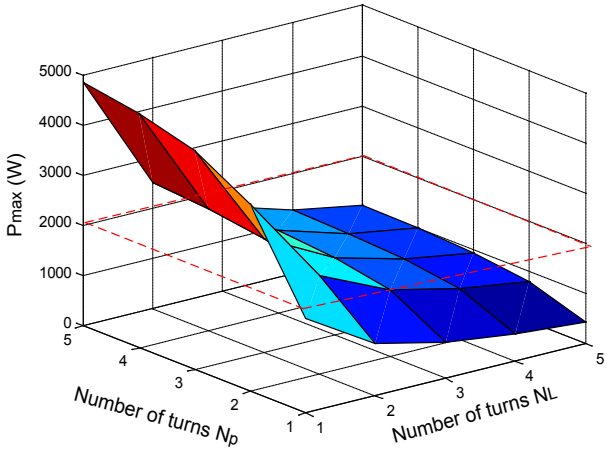

Fig. 5. 3D plot of maximum output power capability.

$\hat{B}_T$ and $\hat{B}_L$ represent the peak flux density of each transformer (T_1 or T_2) and inductor (L_1 or L_2) respectively. $\hat{B}_{Lac}$ is the peak flux density of ac component of each inductor as shown in Fig.9. The same number of primary turns for the two transformers, N_1=N_2=N, is assumed. D is the switching duty cycle, n is the turns ratio of transformers, f is the switching frequency, A_e is the cross-section of the outer leg of E-core, l_g is the length of air gap in each center leg, P_o is the output power, η is the efficiency of the converter, μ_0 is the permeability of air and V_{in} represents the input voltage. In order to avoid flux saturation in the PIM module, the following equations are required,

$$\hat{B}_T + \hat{B}_L = \frac{V_{out} \cdot (1-D)}{4 \cdot n \cdot f \cdot N \cdot A_e} + \frac{\mu_0 \cdot N_L \cdot P_0}{\eta \cdot V_{in} \cdot l_g} + \frac{V_{in} \cdot (D-0.5)}{2 \cdot f \cdot N_L \cdot A_e} \leq B_{sat} \tag{11}$$

The 3D graph in Fig.5 shows the relationship among the output power P_o, the number of turns of primary winding N_P, and the number of turns of inductor winding N_L which has been plotted based on (11) with 100 kHz switching frequency and 0.5 mm airgap. In order to design a 2-kW PIM module, the number of inductor turns, N_L, cannot exceed 3 turns. Its 2D relationship of N_P and N_L corresponding to the maximum output power capabilities is illustrated in Fig.6. The maximum output power can be enhanced by increasing the number of primary turns N or decreasing the number of inductor turns N_L. Fig.7 illustrates the

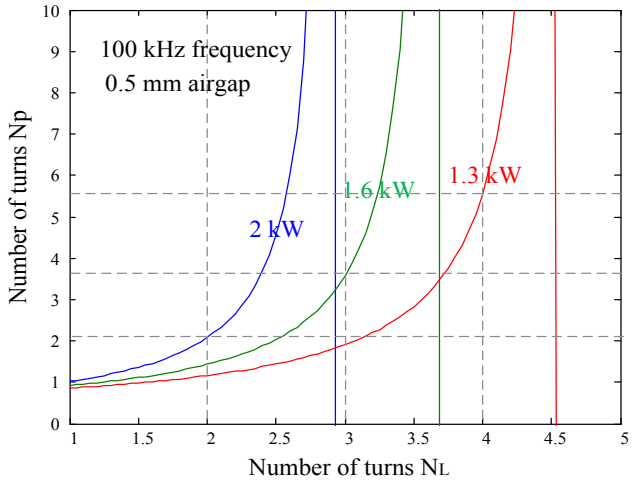

Fig. 6. Relationship of N_L and N_P under different output powers.

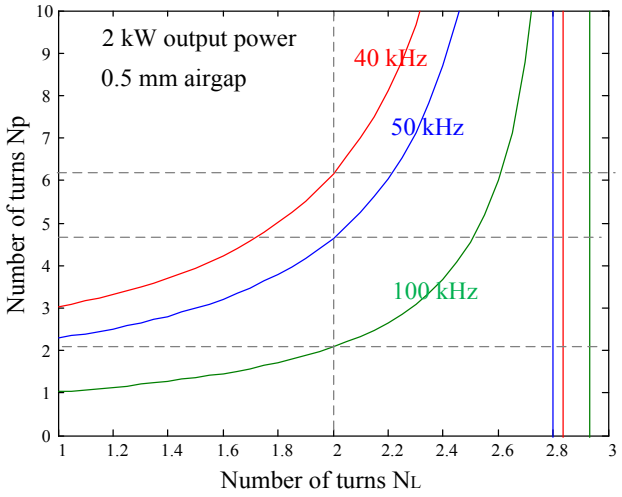

Fig. 7. Relationship of N_L and N_P under different switching frequencies.

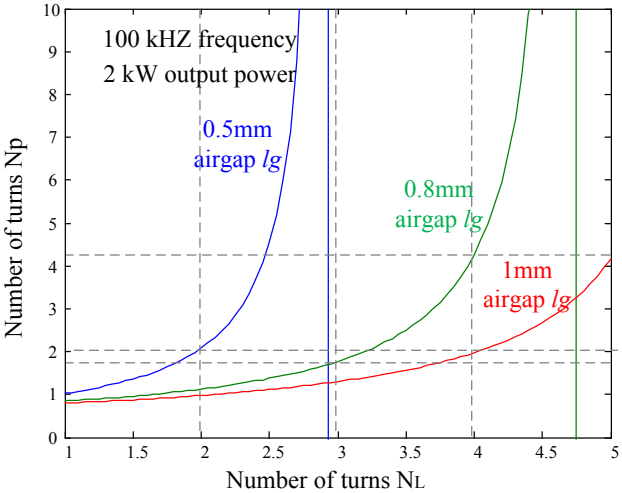

Fig. 8. Relationship of N_L and N_P under different airgaps

fact that maximum output power capability of the PIM module is decreased by reducing the switching frequency. Of course, more energy can be stored by using large airgap, resulting in a large output power capability for the PIM module as illustrated in Fig.8. However, a large airgap results in a low inductance which causes a high current ripple in the circuit for the same number of turns and thereby reduces the efficiency. Moreover, a larger

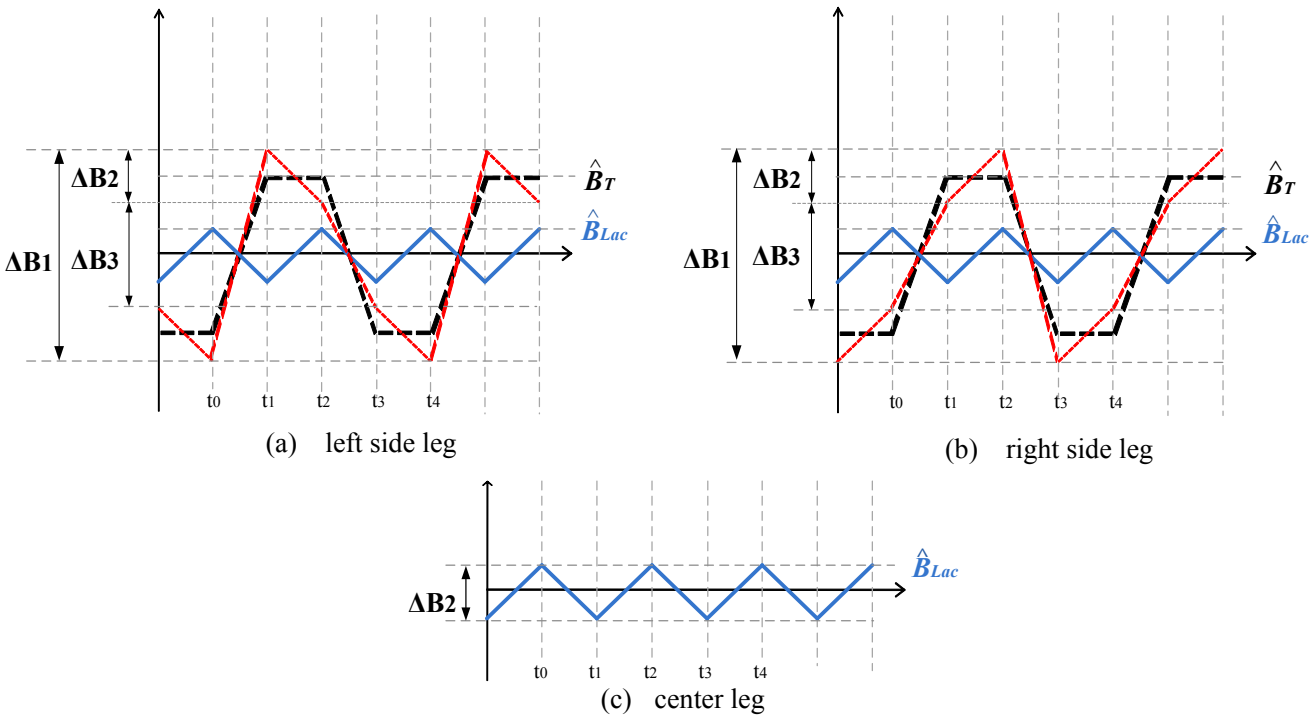

Fig. 9. Flux density waveforms in each leg of the PIM module.

winding loss will be induced due to the fringing effect. Although the maximum output power can also be increased by using higher number of turns of primary winding N, larger winding losses and leakage inductances of the transformers T_1 and T_2 will be produced, reducing the efficiency as well. Unavoidable tradeoff in the power loss exists in the PIM design and the detailed power losses analysis will be given in section V.

V. Power Loss Analysis

A. Core Loss

Core loss separation approach [28] assumes that three fundamental effects are contributing to core losses: static hysteresis loss, eddy current loss and excess eddy current loss. The approach of loss separation has a practical disadvantage: such models are based on parameters, which are not always available and difficult to extract. The most commonly used equation that characterizes core losses is the Steinmetz equation (SE), a curve-fitting expression of measured data under sinusoidal excitation.

$$P_v = k \cdot f^{\alpha} \cdot (\frac{\Delta B}{2})^{\beta} \tag{12}$$

where k, α, β are material parameters , ΔB is peak-to-peak flux density of a sinusoidal excitation with switching frequency f, P_v is time-average core loss per unit volume. Unfortunately, the Steinmetz equation is only valid for sinusoidal excitation. This is a significant drawback since in power electronics applications the core material is normally exposed to non-sinusoidal flux waveforms. Core loss due to non-sinusoidal waveforms can far exceed the loss due to sinusoidal waveforms, even if the frequencies and the peak-to-peak flux densities are identical [29]. In order to determine losses for a wider variety of waveforms, some modified expressions including modified Steinmetz expression (MSE) [30], generalized Steinmetz equation (GSE) [31], improved GSE (IGSE) [32], improved IGSE (I^{2}GSE) [33], natural Steinmetz extension (NSE) [34], equivalent elliptical loop (EEL) [35] and waveform coefficient Steinmetz equation (WCSE) [36] were introduced. A complete comparison among these modified empirical methods shows that the IGSE have the best loss determination with a wide variety of waveforms [29].

$$P_v = \frac{1}{T} \cdot \int_0^T k_i \cdot \left|\frac{dB(t)}{dt}\right|^{\alpha} \cdot \Delta B^{\beta-\alpha} \cdot dt \tag{13}$$

where,

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \cdot \int_0^{2\pi} |\cos\theta|^{\alpha} \cdot 2^{\beta-\alpha} \cdot d\theta}$$

(13) shows the IGSE expression where k, α and β are the same parameters used in the Steinmetz equation (12). The angle θ represents the phase angle of the sinusoidal waveform. Applying a piecewise linear model (PWL) to any waveform and then combining with the IGSE, leads to an easy-to-use expression for accurate calculation of losses with any flux waveform, without requiring extra characterization of material parameters beyond the parameters of the Steinmetz equation.

It is necessary to know the flux density waveforms to estimate core loss properly using IGSE. Fig.9 shows the flux density waveforms in each leg of the PIM module.

1) In the time period t_0~t_1, the transformer flux Φ_T and the inductor flux Φ_L are adding together in the left side legs of both E-cores. On the other hand, they are cancelling in the right side legs.

2) During the time period t_1~t_2, the rate of change of Φ_T is zero, and therefore ac flux ΔB_2 in the two side legs are identical to ac flux on the inductor ΔB_L.

3) t_2~t_3, is the opposite of the period t_0~t_1 where the transformer flux Φ_T and the inductor flux Φ_L are opposing in the left side legs of both E-cores. Meanwhile, they are added in the

TABLE II
CALCULATED RESULTS FOR CORE LOSS WITHOUT PRE-MAGNETIZATION

Input voltage	Core loss			
	Left side leg P_{CL}	Right side leg P_{CR}	Center leg P_{CC}	Total
V_{in}=30 V	5.95 W	5.95 W	0.09 W	12 W
V_{in}=45 V	13.43 W	13.43 W	0.01 W	26.87 W

TABLE III
ERROR ANALYSIS BETWEEN NORMAL STEINMETZ EQUATION AND IMPROVED STEINMETZ EQUATION

		SE with eqn. (12)	IGSE with eqn. (13)	Error
V_{in}=30 V	Left side leg P_{CL}	3.47 W	5.95 W	42%
	Right side leg P_{CR}	3.47 W	5.95 W	42%
	Center leg P_{CC}	0.01 W	0.09 W	90%
V_{in}=45 V	Left side leg P_{CL}	7.9 W	13.43 W	42%
	Right side leg P_{CR}	7.9 W	13.43 W	42%
	Center leg P_{CC}	0.001 W	0.01 W	90%

right side legs.

4) t_3~t_4, is the same as t_1~t_2. The red dashed lines shown in Fig.9 (a) and Fig.9 (b) represent the overall flux density waveforms in the two side legs respectively. Since the flux of transformer Φ_T does not go through the center leg, the overall flux density waveform in the center leg is only dependent on the flux of inductor Φ_L.

The core loss can be calculated individually for each leg. For the applied flux waveform as illustrated in Fig.9, by using (13) together with PWL method, the following equations of core loss for each leg is obtained,

$$P_{vs} = k_i \cdot f^{\alpha} \cdot [(\Delta {B_1}^{\beta} + \Delta {B_3}^{\beta}) \cdot (1-D)^{1-\alpha} + 2 \cdot \Delta {B_2}^{\beta} \cdot (D-0.5)^{1-\alpha}] \tag{14}$$

$$P_{vc} = 4 \cdot k_i \cdot f^{\alpha} \cdot \Delta {B_2}^{\beta} \cdot (D-0.5)^{1-\alpha} \tag{15}$$

where,

$$\Delta B_1 = 2 \cdot (\hat{B}_T + \hat{B}_{Lac})$$

$$\Delta B_2 = 2 \cdot \hat{B}_{Lac}$$

$$\Delta B_3 = \Delta B_1 - \Delta B_2 = 2 \cdot (\hat{B}_T - \hat{B}_{Lac})$$

and P_{vs} is the core loss per unit volume in each side leg and P_{vc} is the core loss per unit volume in the center leg. The flux Φ_1 is identical to the flux Φ_2 due to two transformers operating with in-phase currents utilizing the same control signals. The two flux Φ_1 and Φ_2 are fully cancelled in the shared I-core where zero core loss ideally can be achieved. Table II shows the calculated results of core loss in each leg with different input voltages. The worst case for the core loss is in high input voltage where a higher peak flux is induced. In order to illustrate the inaccuracy of SE with (12), Table III shows an error analysis between SE and IGSE for the core loss of the PIM module.

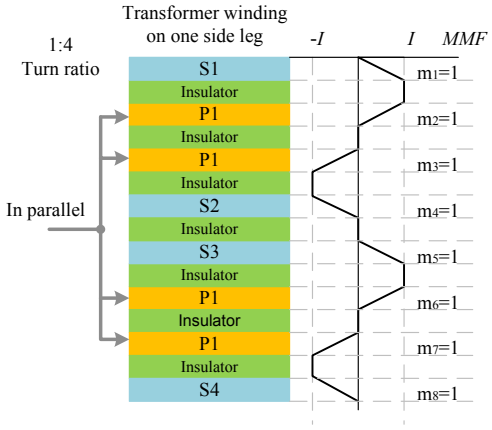

Fig. 10. Winding arrangement and MMF distribution for the transformer windings wound on one of the outer legs.

However, the aforementioned calculations are based on the IGSE formula which neglects the fact that core losses vary under dc bias conditions, i.e. the Steinmetz parameters change under dc bias condition. When a core operates under dc bias condition, the core loss still can be described using the Steinmetz equation (12) or the IGSE (13). However, the Steinmetz parameters must be adjusted according to the dc bias present. Pre-magnetization H_{DC} causes changes in the Steinmetz parameters β and k_i, but not in the parameter α. For many materials, the impact of a dc bias cannot be neglected as it may increase the core loss by a factor of more than two [37]. According to Steinmetz Pre-magnetization Graph (SPG) of the material ferrite N87 in [37], the core losses in this converter under different dc bias can be approximately estimated by multiplying the coefficient of SPG. The results are shown in Table VI and Table VII respectively.

B. *Winding Loss*

Winding losses in transformers increase dramatically with high frequency due to eddy current effects. Eddy current losses, including skin effect and proximity effect losses seriously impair the performance of transformers in high-frequency power conversion applications. Both the skin effect and the proximity effect cause the current density to be non-uniformly distributed in the cross-section of the conductor, and thus cause a higher winding resistance at higher frequency. The most commonly used equation that characterizes winding losses is the Dowell's equation [38]-[40],

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\varepsilon}{2} \cdot \left[\frac{\sinh\varepsilon + \sin\varepsilon}{\cosh\varepsilon - \cos\varepsilon} + (2m-1)^2 \cdot \frac{\sinh\varepsilon - \sin\varepsilon}{\cosh\varepsilon + \cos\varepsilon}\right] \tag{16}$$

where ε is the ratio of copper thickness h to the skin depth δ in a given frequency, and m is defined as a ratio in (17),

$$m = \frac{F(h)}{F(h) - F(0)} \tag{17}$$

where $F(0)$ and $F(h)$ are magneto motive forces (MMFs) at the limits of a layer as shown in Fig.10. The first term in (16) describes the skin effect and the second term represents the proximity effect. The proximity effect loss, in a multilayer

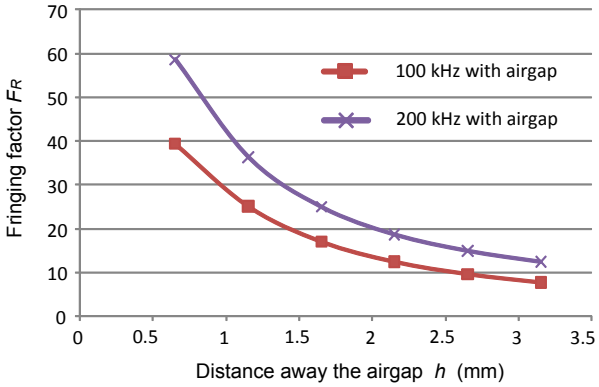

Fig. 11. Fringing factor F_R with different winding locations.

winding, may strongly dominate over the skin effect loss depending on the winding arrangement [40]. Interleaving transformer windings may reduce the proximity loss significantly when the primary and secondary currents are in-phase [41]. Similarly, the leakage inductance of a transformer can also be significantly reduced [42]. Fig.10 shows the winding arrangements and MMF distributions along the vertical direction for the windings of transformer T_1 or T_2 wound on one of the outer legs. The MMF ratio m for each layer is equal to 1 which results in a lower ac resistance and leakage inductance. As seen in (16), ac resistance is not only related to MMF ratio m, but also to the ratio ε. A thinner copper can minimize the eddy current effect but a higher dc resistance will be compromised. Therefore, for a given frequency and winding arrangement, minimum ac resistance can be obtained by selection of proper copper thickness. Considering the cost of PCB and manufacturing simplicity, a 4-oz PCB copper thickness has been chosen for both primary and secondary windings for the experiment in this paper. In practice, PCB winding has a larger resistance compared to the calculation due to PCB vias and the fabrication tolerances.

It is noted that the validity of the expression (16) relies on negligible distances between consecutive turns, between adjacent layers, between the conductor edge and the magnetic core. Furthermore, the expression (16) is only valid for sinusoidal excitation waveform. Winding loss calculation for any current waveform to correct Dowell's assumptions can be found in [39]. Also [43] gives generalized correction factors to be applied to Dowell's resistance factor expression. However, these factors are usually derived from elaborated formulas and have to be determined from complicated coefficient tables.

Ferrite core has a limited saturation flux density, which requires inclusion of an airgap in the magnetic path in order to store energy for the inductors L_1 and L_2. A large airgap results in fringing flux which has two effects. First, the inductance is increased due to the effective increase in the airgap cross-sectional area, which decreases the reluctance of the gap. Second, the fringing flux induces eddy currents in the surface of nearby conductors, which causes a higher ac resistance and thereby increases the conduction loss. The fringing effect can be expressed as follows,

$$R_{ac} = F_R \cdot R_{dc} \tag{18}$$

where F_R represents the factor of fringing effect. Dowell's equation (16) does not include the fringing effect caused by the airgap. Therefore F_R in this case is much higher than the one

TABLE IV
SWITCHING LOSS PARAMETERS

Parameters	Values
Clamp voltage, V_C	84 V (at 100˚C)
Gate to source voltage at $V_{GS}(i_s)$	4.1 V
Common source inductance, L_{CS}	11.3 nH
Stay and leakage inductance, L_X	52.7 nH

calculated by Dowell's equation. How the fringing field affects the high frequency winding loss and how to configure the windings to minimize the effect of the fringing field of the air gap have been investigated recently in [44]-[45]. The PCB windings are kept far away from the airgap in order to minimize the fringing effect in this work. The fringing effect in the PIM module has been considered by using FEA simulation tool. Fig.11 shows FEA simulation results of the fringing effect of an airgap at different windings locations. Almost 60 times of dc resistance can be obtained when the windings are close to the airgap and with 200 kHz inductor current ripple.

C. Switching Loss of MOSFETs

Hard switching isolated dc-dc converters suffer increased switching loss due to leakage and stray inductances of the isolation transformer and layout, respectively. Both precise calculation and measurement of the switching losses are not straightforward due to voltage dependant parameters of the MOSFTEs like the output capacitor and time scale mismatch of MOSFET drain current and voltage waveforms. MOSFETs used in boost-type isolated dc-dc converters experience inductive switching since neither the input nor the output capacitors can directly clamp their drain-to-source voltages. This condition results in switching spikes occurring on top of the drain-to-source voltage during the turn-off process [46].

During turn-off, drain-to-source capacitance voltage of the MOSFET rises with a speed determined by the current sinking capability of the gate driver circuit in order to charge the Miller capacitance. Mostly this charging is lossless when performed by an inductive element which is the case in boost type converters. However during the turn-on process the stored energy in the output capacitor of the MOSFET is dissipated. This loss may become significant in higher voltage and frequency levels.

Apart from the capacitive switching loss considerations, additional factors come into play in high input current dc/dc applications. Common source inductance (Fig.12) and gate driver voltage become the limiting factors for the MOSFET current turn off speed [47]. The negative rate of change of the drain current during turn-off induces a positive gate-to-source voltage which

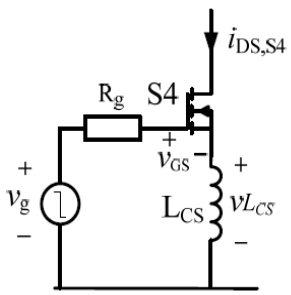

Fig. 12. Common source inductance acting as additional voltage in the gate driver circuit.

TABLE V
MAGNETIC PARAMETERS OF PIM MODULE

Parameters	Values
Number of turns in primary (N_1=N_2)	2
Turns ratio of each transformer	1:4
Number of turns for the inductors (N_{L1}=N_{L2})	2
Each air gap length (lg)	0.5 mm
Core type	EILP 64
Core material	Ferrite N87
Copper thickness mount on PCB layer	4 oz (140 µm)
Switching frequency	100 kHz

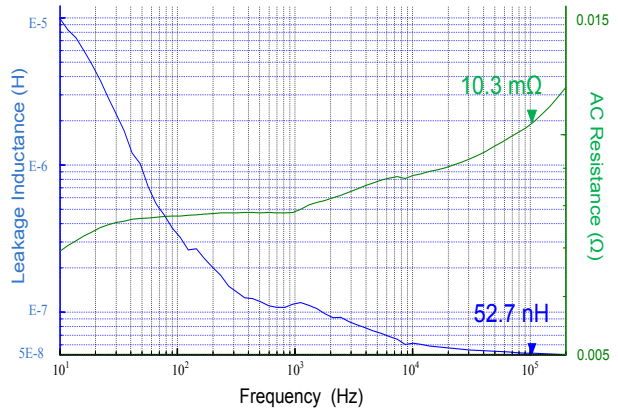

Fig. 13. Measurement results of impedance. (a) transformer T_1 or T_2. (b) Inductor L_1 or L_2.

may keep the MOSFET in its active region together with a high drain-to-source voltage. So this extra voltage will behave as a negative feedback in the switching seep, putting an upper limit to it. A detailed analysis on two commutation types, namely voltage limited and MOSFET limited commutations, during the turn-off of MOSFET is obtained in [46]. The boundary expression determining the commutation mode is,

$$\frac{L_X}{L_{CS}} = \left(V_C - \frac{V_0}{2n}\right) \cdot \left(\frac{1}{2 \cdot V_{GS}(i_s)} + \frac{2n}{V_0}\right) \tag{19}$$

where L_X is composed of the leakage inductance and stray inductance due to the converter layout. L_{CS} is the common source

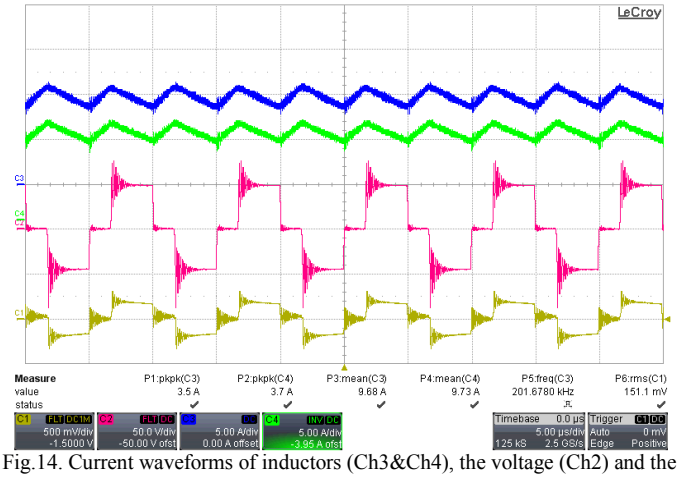

Fig.14. Current waveforms of inductors (Ch3&Ch4), the voltage (Ch2) and the current (Ch1) of T_1.

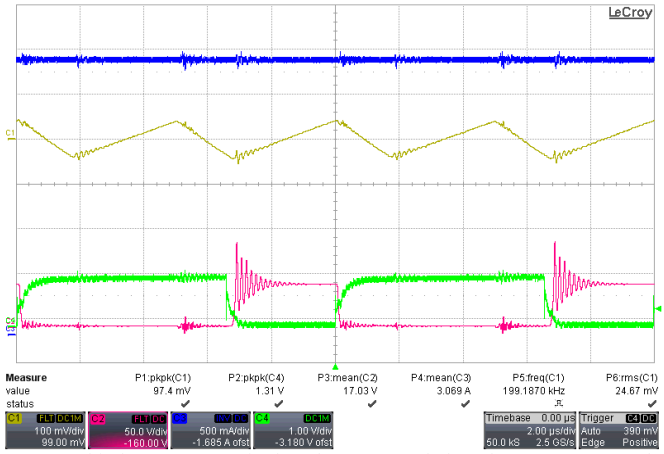

Fig.15. Total inductor current ripple (Ch1, AC coupled) and output current (Ch3), V_{DS} (Ch2) and V_{GS} (Ch4) of S_1.

inductance including the internal package inductance and the package source pin inductance. $V_{GS}(i_s)$ is the gate voltage corresponding to the drain at the start of the turn-off process. V_C is the clamp voltage which may be provided by an external clamp circuit or the avalanche voltage of the MOSFET. Table IV shows the corresponding values of these parameters used in this paper. In order to have a practical value for L_{CS}, 7 *nH/cm* rule of thumb has been used. The stay and leakage inductance L_X can be found in the measurement results of Section VI. The condition in (19) can be tested for this case by inserting the parameters of Table IV which results in,

$$\frac{L_X}{L_{CS}} < \left(V_C - \frac{V_0}{2n}\right) \cdot \left(\frac{1}{2 \cdot V_{GS}(i_s)} + \frac{2n}{V_0}\right).$$

This result confirms the commutation mode as MOSFET limited commutation as explained in [1]. Therefore, in this case the expression for the switching losses per full bridge is,

$$P_s = f \cdot \left[1 + \frac{V_0}{4 \cdot n \cdot V_{GS}(i_s)} \cdot L_{CS} + L_X\right] \cdot {I_{Lpeak}}^2 \tag{20}$$

VI. EXPERIMENTAL RESULTS

A. Results of PIM module

A 2-kW prototype has been built to verify the new integrated magnetics design approach. Input voltage is between 20-50 V

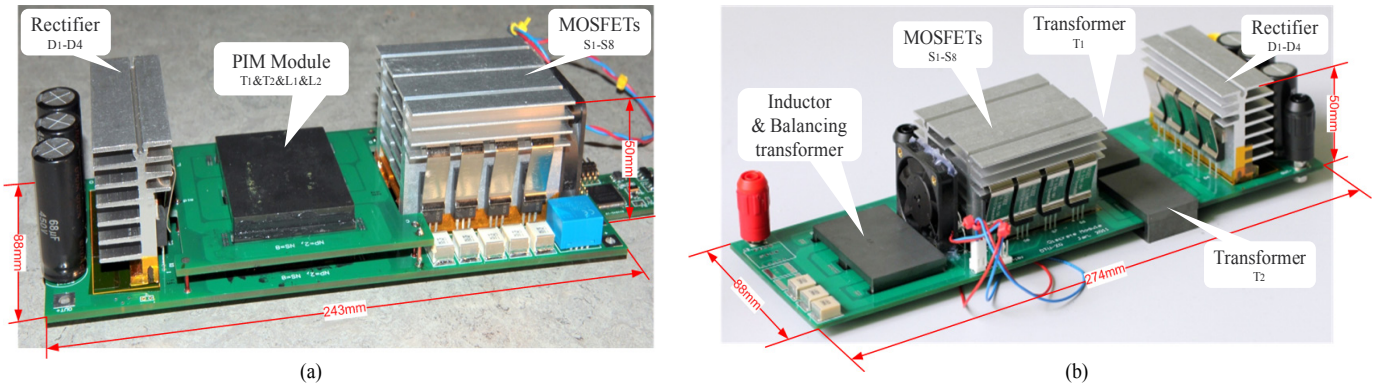

Fig. 16. Photo of experimental prototype converters (a) with PIM module (b) with single inductor, integrated balancing transformers and discrete transformers.

TABLE VI

CONVERTER POWER LOSS BREAKDOWN AT 45-V INPUT, 400-V OUTPUT AND 1.5-KW OUTPUT POWER

Components	Loss Type		Loss (W)
PIM module	Winding loss	T_1&T_2	5.2 W
		L_1&L_2	2.0 W
	Core loss		37.8 W
MOSFET 8 pcs.	Conduction		2.3 W
	Switching Loss		9.9 W
Diodes 4 pcs.	Conduction		5.9 W
	Switching Loss		1.8 W
Total loss			64.9 W

TABLE VII

CONVERTER POWER LOSS BREAKDOWN AT 30-V INPUT, 400-V OUTPUT AND 1.5-KW OUTPUT POWER

Components	Loss Type		Loss (W)
PIM module	Winding loss	T_1&T_2	7.9 W
		L_1&L_2	5.3 W
	Core loss		22 W
MOSFET 8 pcs.	Conduction		4.6 W
	Switching Loss		22 W
Diodes 4 pcs.	Conduction		7.9 W
	Switching Loss		2.3 W
Total loss			67.7 W

and output voltage is 400 V. Primary switches are IPA028N08N3, 80-V, 2.8-mΩ power MOSFETs from Infineon. Output rectification is handled by Silicon Carbide Schottky diodes C3D10060A with 1.5-V forward voltage drop. Magnetic parameters of the PIM module are shown in Table V. One set of EELP-64 core and an additional piece of I-64 core, all composed of N87 core material. The core material selection is directly related to the core loss. In order to feature a lower core loss, ferrite materials are usually chosen as a suitable transformer's core material operating around hundreds kilo-hertz. Each transformer turns ratio is 1:4 (n=4). Air gaps with 0.5-mm length are used for the energy storage inductors L_1 and L_2. 4-oz copper thickness is used for PCB windings. Switching frequency is 100-kHz with inductor current ripple of 200-kHz. The frequency selection does not affect the integrated operation principle and the same advantages for the PIM module are achieved regardless of the frequency. And the size of converter can be further reduced if a high frequency is selected. But it is note that the frequency selection is related to the optimization design. Higher frequency may cause a higher power loss due to a high frequency eddy current effect in the windings, higher core loss in the magnetic material and higher switching loss of power MOSFETs. In addition, higher frequency causes a higher maximum output capability of the PIM module (PIM module can be operated under a high power level if a high frequency is selected).

Interleaved winding technique shown in Fig.10 is utilized to reduce the ac resistances and the leakage inductances. The measurement results for the integrated transformers and inductors are shown in Fig.13, obtained by PSM1735, impedance analyzer. The ac resistance and leakage inductance are obtained by opening secondary side and shorting both primary sides. The results in the figure have been referred to the primary side. Assuming that T_1 and T_2 have the same parameters, 52.7-nH leakage inductance and 10.3-mΩ ac resistance referred to the primary sides of each transformer can be derived. The stray parameters of the circuit are also included in the measurement results. Keeping the PCB winding far to the airgap, the fringing effect of airgap causes ac resistance of the inductors, L_1 and L_2, is 16.4 times than their dc resistances. The ac resistance of each inductor is 55.6-mΩ when the inductor current ripple works at 200-kHz. According to the above measurement results, detailed breakdown of power losses for 1.5-kW PIM module at 45-V input and 30-V input can be found in Table VI and Table VII respectively. The core loss of PIM dominates over the total power loss especially for high input voltage like 45-V. The winding loss of PIM is far less than the core loss which may not an optimization case. The solution for this is to balance the core loss and winding loss by increasing the number of turns of primary. However, it is noted that the fully interleaving may not be implemented due to the PCB layer limitation; otherwise the cost of PCB manufacture will be extremely high. The switching loss dominates over the total power loss when the converter operates at low voltage input like 30-V. As seen from (20), the

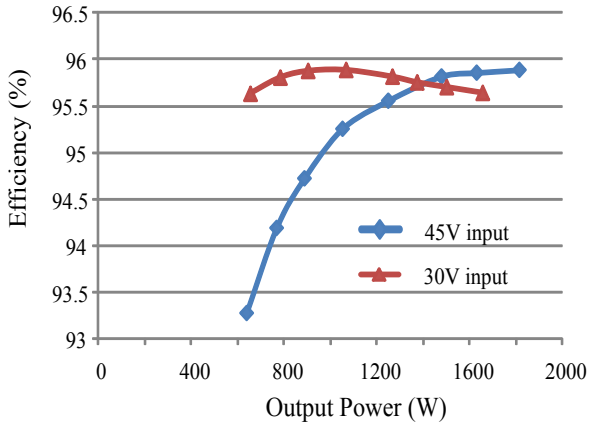

Fig. 17. Measured converter efficiency for PIM dc-dc converter.

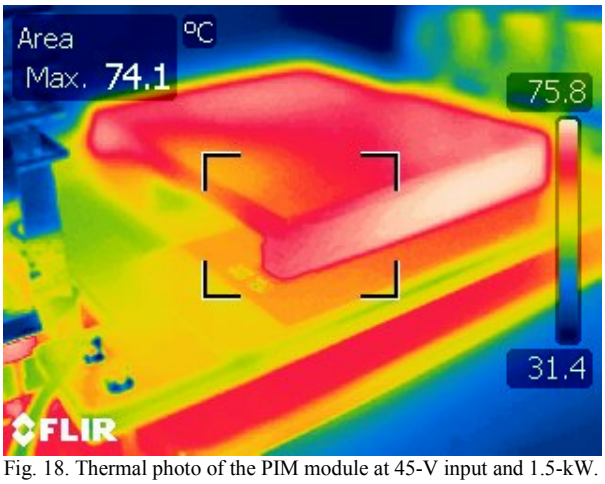

Fig. 18. Thermal photo of the PIM module at 45-V input and 1.5-kW.

leakage inductance and stay inductance become very important in low voltage case. With the aforementioned solution of increased number of primary turns, the leakage inductance will be increased which allows a very high switching loss. Therefore, many tradeoffs exist in the PIM module and an optimization procedure needs to be done. However, this paper emphasis on the integration approach, the proof-concept demonstration rather than the optimization design.

IRS2110 high and low side gate drivers are used in the gate driver circuit together with ISO722C capacitive digital isolators for control signal protection. The control signals are produced by TMS28027 DSP. Fig.16-(a) shows the experimental prototype employing the proposed PIM module. Output is filtered by several 1-uF SMD capacitors in parallel placed very close to the rectifiers for minimizing the ac loop. When the converter operates at 100-kHz, 30-V input, 400-V output and 1.5-kW output power, the current waveforms of inductors (Ch3&Ch4), the voltage (Ch2) and the current (Ch1) of transformer T_1 are presented in Fig.14. Observe that the two currents are identical. Removing oscilloscope offset, causes current traces to fully coincide. Also the total inductor current ripple (Ch1, AC coupled) and output current (Ch3), V_{DS} (Ch2) and V_{GS} (Ch4) of S_1 are shown in Fig.15 respectively.

High stability (< 10 ppm) 0.1 % shunt resistors are used for high precision of the efficiency measurements. Agilent 34410A high precision multimeters are used for all measurements. Current sense signals are shielded and fitted with common mode filters. Efficiency curves of the converter employing the PIM

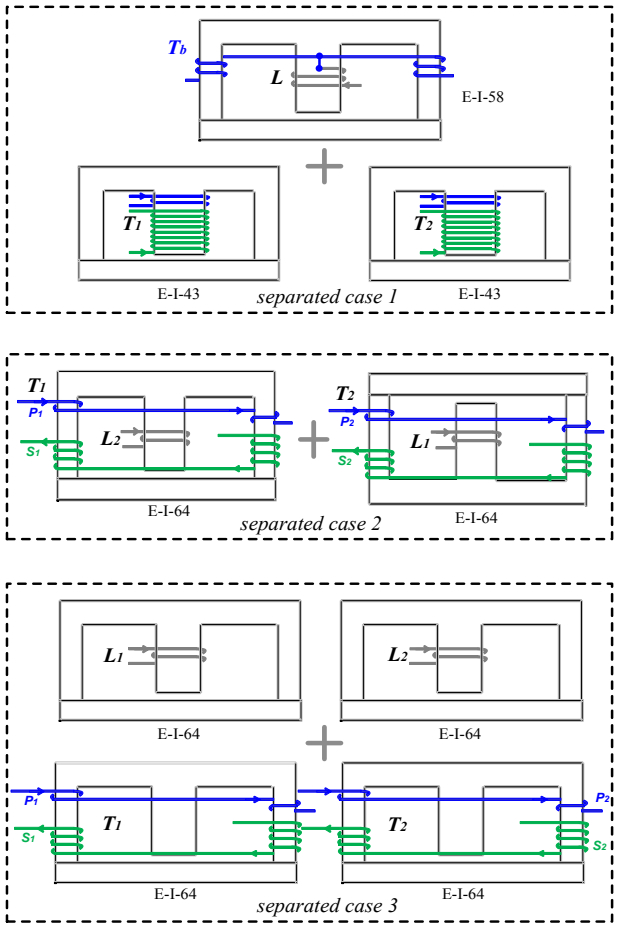

Fig. 19. Separated cases for experimental comparisons.

module when the output voltage is 400-V are shown in Fig.17. Maximum efficiency of 95.9% has been observed with 45-V input voltage, 400-V output voltage and 1.8-kW output power. And the same maximum efficiency can be observed at 30-V input voltage, 400-V output voltage and 1-kW. In low output power, the efficiency of 30-V input is much higher than that of 45-V input this is due to the fact that the low number of primary turns in this case causes the core loss of PIM dominating over the total power loss which has been mentioned in the previous. With increased output power, the switching loss becomes a crucial part in total power loss. Therefore, a lower efficiency at 30-V input can be observed. Fig. 18 shows a thermal photo of PIM module at 45-V and 1.5-kW in which is the worst case for the core loss. Notice that a forced air flow from fan is used for cooling down the converter. As shown in the photo, the heat mostly concentrates on the side legs rather than the center leg. This is coincident with the analysis of core loss in section V.

B. Comparison

In order to demonstrate the advantages of PIM such as low profile and high efficiency, a comparison between the PIM and three different separated cases has been done. In order to make a fair comparison, all switching devices, gate drivers, and capacitors are kept the same. The prototype of separated case-1 is shown in Fig.16-(b) which is consisted of single inductor with integrated balancing transformers and two discrete transformers. The detailed principle about this structure can be found in [26]. In separated case-1, two turns single inductor are wound in EILP-58 core with 0.5-mm airgap length and two turns of integrated balancing transformer are wound in each side leg. The

TABLE VIII

POWER LOSS BREAKDOWN OF SEPARATED CASE-1 CONVERTER AT 45-V INPUT, 400-V OUTPUT AND 1.5-KW OUTPUT POWER

Components	**Loss Type**		**Loss (W)**
PIM module	Winding loss	T_1&T_2	14.8 W
		L_l&T_b	8.2 W
	Core loss		28.5 W
MOSFET 8 pcs.	Conduction		6.4 W
	Switching Loss		17.8 W
Diodes 4 pcs.	Conduction		7.4 W
	Switching Loss		3.7 W
Total loss			86.8W

two discrete transformers are both employing EILP-43 cores with two turns in primary sides and 8 turns in secondary sides. N87 core material is used for all cores in the separated case-1. And full interleaved winding arrangement is also used in this case. The separated case-2 is partially using integrated technology shown in Fig.19. The PCB winding and core size are kept the same with PIM module. Two E-I cores have been separated by adding a single I-core on the basis of PIM module. A single inductor and a single transformer are still integrated into the E-I core. A complete separation has been implemented in the separated case-3, consisting of four discrete magnetic components, L_1, L_2, T_1 *and* T_2. And the windings of transformer still keep the same arrangements with PIM module shown in Fig.19. The two inductors and two transformers are using the same core geometry EILP-64. Obviously, the PIM module has the smallest footprint and fewest numbers of components compared to the other separated cases. Fig.20 and Fig.21 show the efficiency comparisons among the four cases at 45-V input and 30-V input respectively. Regarding to the power losses of the separate case-2 and case-3, the only difference with PIM case is to have higher core loss. This is because the flux is cancelled in the shared I-core in PIM case, causing a lower core loss. Winding layouts are not changed and thus the other power losses are kept the same with PIM case. From the efficiency curves, the case-2 and case-3 almost have the same core loss at 45-V input and the PIM has 1% improvement at 1.5-kW output power. When the input voltage is 30-V, the efficiency of the separated case-3 is slightly higher than that of the case-2. The PIM case has almost 0.5% improvement at 1.5-kW output power. Regarding to the separated case-1, some design parameters including the number of turns of integrated balancing transformers, the winding widths, the winding lengths, the winding arrangements and the core geometries are different with the PIM case. Therefore, the difference in power loss between the PIM case and the case-1 is not only the core loss, but also the winding loss and the switching loss. The power loss breakdown for separated case-1 is shown in Table VIII. From the efficiency figures, the separated case-1 has lower efficiencies than the PIM case at nominal output power. Notice that the comparison between the PIM case and separated case-1 is not fair since the two cases are both not optimized. And the efficiency of separated case-1 might be improved by changing winding widths and winding

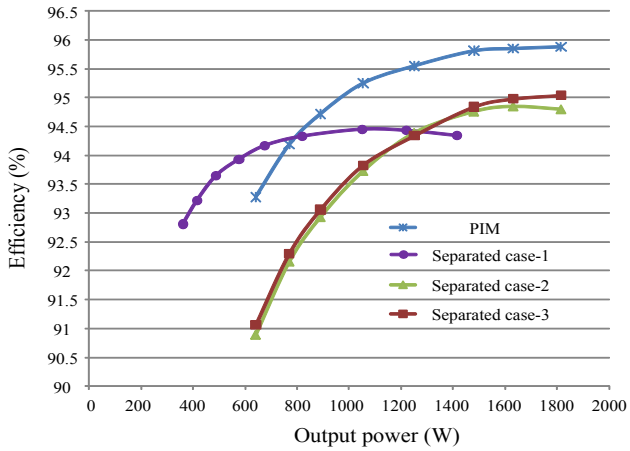

Fig. 20. Efficiency comparison at 45-V input and 400-V output.

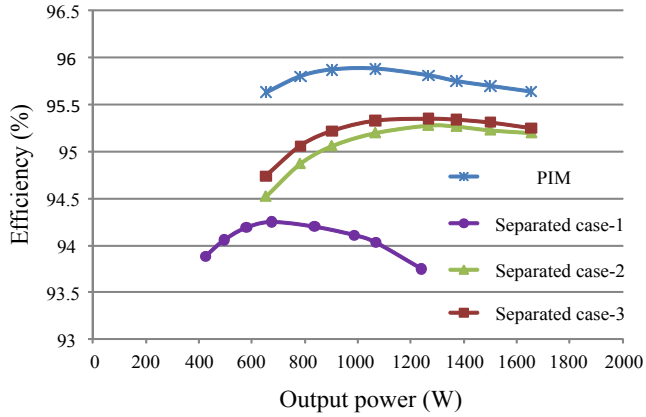

Fig. 21. Efficiency comparison at 30-V input and 400-V output.

arrangements and enhancing the value of inductor. Larger core geometries could also be used for the efficiency improvement. However, the power density (larger core geometries) and the cost (more PCB layers for higher inductance) will be lost if the aforementioned methods are used.

VII. Conclusion

This work presents a new integrated magnetics approach to combine all magnetic components of the primary-parallel isolated boost converter into an E-I-E core structure. Since the design approach allows the transformers and inductors are electromagnetically uncoupled, it can be extended into many other isolated dc-dc topologies where multiple transformers and multiple inductors are involved in. The similar matter results are achieved for the extended topologies and all the advantages aforementioned will not be losing. The design approach provides a low footprint, low cost and high efficiency. Also, the integrated magnetics with planar components are made from pre-formed assemblies, thus the assembly process itself has only a few stages. This simplification of assembly allows the PIM to be manufactured with very high repeatability and with increased accuracy. The drawback of the PIM module is to limit the maximum the output power capability due to the overlapped flux. The detailed limitation of power capability has been presented and analyzed. Power loss analysis of the converter has been investigated in-depth. Test results from a 2-kW experimental prototype verify that converter employing the PIM module is fully functional and electromagnetically equivalent. An

efficiency of 95.9% can be achieved during 1.5-kW nominal operating conditions. Experimental comparisons between the PIM module and three separated cases have illustrated the PIM module has advantages of lower footprint and higher efficiencies.

APPENDIX

In this appendix it is shown that the two transformers T_1 and T_2 have a partial coupling effect. The equivalent magnetic reluctance model between T_1 and T_2 is shown in the bottom of Fig.4.

$$N_1 \cdot i_{m1} = \Phi_1 \cdot (2R_1 + R_2) + (\Phi_1 - \Phi_2) \cdot R_2 \tag{21}$$

$$N_2 \cdot i_{m2} = \Phi_2 \cdot (2R_1 + R_2) + (\Phi_2 - \Phi_1) \cdot R_2 \tag{22}$$

Combining (21) and (22), the following equations are obtained,

$$\Phi_1 = \frac{2 \cdot N_1 \cdot (R_1 + R_2)}{\Delta} \cdot i_{m1} + \frac{N_2 \cdot R_2}{\Delta} \cdot i_{m2} \tag{23}$$

$$\Phi_2 = \frac{N_1 \cdot R_2}{\Delta} \cdot i_{m1} + \frac{2 \cdot N_2 \cdot (R_1 + R_2)}{\Delta} \cdot i_{m2} \tag{24}$$

where

$$\Delta = 4 \cdot {R_1}^2 + 8 \cdot R_1 \cdot R_2 + 3 \cdot {R_2}^2$$

Taking the partial derivative in (23) and (24),

$$N_1 \cdot \frac{d\Phi_1}{dt} = \frac{2 \cdot {N_1}^2 \cdot (R_1 + R_2)}{\Delta} \cdot \frac{di_{m1}}{dt} + \frac{N_1 \cdot N_2 \cdot R_2}{\Delta} \cdot \frac{di_{m2}}{dt} \tag{25}$$

$$N_2 \cdot \frac{d\Phi_2}{dt} = \frac{N_1 \cdot N_2 \cdot R_2}{\Delta} \cdot \frac{di_{m1}}{dt} + \frac{2 \cdot {N_2}^2 \cdot (R_1 + R_2)}{\Delta} \cdot \frac{di_{m2}}{dt} \tag{26}$$

(27) is rewritten from (25) and (26),

$$\begin{bmatrix} \lambda_1 \\ \lambda_2 \end{bmatrix} = \begin{bmatrix} \frac{2 \cdot {N_1}^2 \cdot (R_1 + R_2)}{\Delta} & \frac{N_1 \cdot N_2 \cdot R_2}{\Delta} \\ \frac{N_1 \cdot N_2 \cdot R_2}{\Delta} & \frac{2 \cdot {N_2}^2 \cdot (R_1 + R_2)}{\Delta} \end{bmatrix} \cdot \begin{bmatrix} i_{m1} \\ i_{m2} \end{bmatrix} = \begin{bmatrix} L_{11} & L_M \\ L_M & L_{22} \end{bmatrix} \cdot \begin{bmatrix} i_{m1} \\ i_{m2} \end{bmatrix} \tag{27}$$

where the flux linkages λ_1 and λ_2 are the time integrals of the transformer primary voltages, i_{m1} and i_{m2} are the individual excitation currents. L_{11} and L_{22} are their self-inductances. L_M represents mutual inductance between the two transformer windings. With assumption that leakage flux through the air is negligible, (28) ~ (30) can be obtained,

$$L_{m1} = L_{11} + L_M = \frac{{N_1}^2}{2 \cdot R_1 + R_2} \tag{28}$$

$$L_{m2} = L_{22} + L_M = \frac{{N_2}^2}{2 \cdot R_1 + R_2} \tag{29}$$

$$k = \frac{L_M}{L_{11}} = \frac{R_2}{2 \cdot (R_1 + R_2)} \tag{30}$$

The results of magnetizing inductance of transformers are the same with that in Section III. k represents the coupling coefficient between T_1 and T_2. According to the geometry of core, k=0.4 can be obtained for their coupling coefficient.

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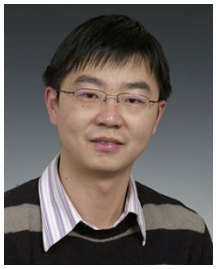

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Appendix A9

[A9] K. L.-Poulsen, Z. Ouyang, **G. Sen**, M. A. E. Andersen, "A new method for start-up of isolated boost converters using magnetic- and winding-integration," in Proc. APEC 2012 (**Published**).

A New Method for Start-up of Isolated Boost Converters Using Magnetic- and Winding-Integration

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***Abstract*—A new solution to the start-up and low output voltage operation of isolated boost family converters is presented. By the use of integrated magnetics and winding integration, the transformer secondary winding is re-used during start-up as a flyback winding coupled to the boost inductor. The traditional added flyback winding coupled to the boost inductor is thus eliminated from the circuit, bringing substantial cost savings, increased efficiency and simplified design. Each subinterval of the converter operation is described through electrical and magnetic circuit diagrams, and the concept is extended to other isolated boost family topologies. The principle of operation is demonstrated with a 800W isolated boost prototype, and a 1600W primary parallel series secondary isolated boost converter. Efficiency measurements of both prototypes are presented, including measurements during both start-up and normal boost operation.**

I. Introduction

Isolated boost converters have been shown to be the most efficient topology for high power, low input voltage, high output voltage applications [1]–[5]. Suitable applications include distributed generation systems, backup systems, fuel cell converters, electric vehicle applications and avionic applications. However, a disadvantage of the topology is that the boost characteristic sets a lower limit for the output voltage, which introduces in-rush current during start-up from zero output voltage, as well as during fault situations such as output short circuit.

Fig.1 shows a common solution to the start-up problem [6], [7]. A flyback winding is arranged on the boost inductor, such that the converter may operate as a flyback converter during start-up with the associated buck-boost voltage modulation factor allowing control of the output voltage all the way down to zero volts. During normal boost operation, the flyback winding is completely inactive, but occupies part of the winding window of the boost inductor, leaving less copper area for the boost inductor, which in turn causes a drop in efficiency. Being a power transferring magnetic component, the flyback winding is a relatively expensive circuit element and complicates the assembly of the boost inductor. Fig.2 and Fig.3 respectively show the simplified and complete circuit diagrams of the new circuit topology, where the magnetic integration of the boost inductor with the transformer allows the boost inductor to couple to the secondary winding during start-up, such that the secondary winding acts as flyback winding.

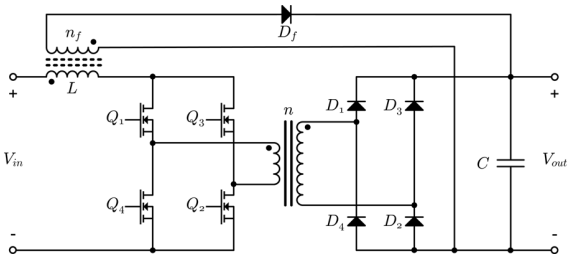


Fig. 1. Isolated full-bridge boost converter with traditional start-up method using added external flyback winding and diode.

II. Principle of Operation

Figures 4 to 7 explain the principle of operation as applied to the basic full-bridge isolated boost topology. Each

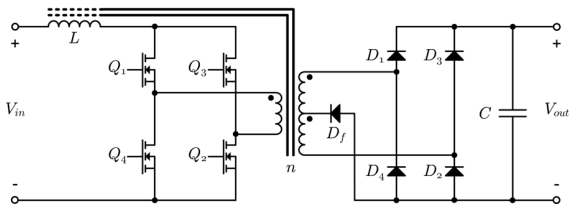


Fig. 2. Electrical circuit diagram of new start-up method.

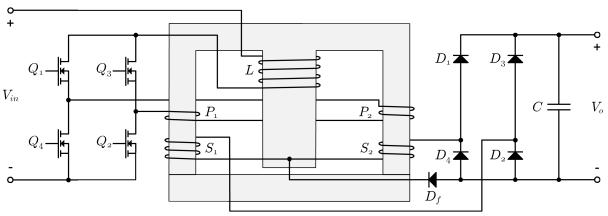


Fig. 3. Electrical and magnetic circuit diagram of new start-up method using EI core with center leg air gap.

subinterval of operation is shown with an electric circuit diagram followed by the corresponding and a magnetic core diagram. Relevant voltage polarities are marked with +/- signs, and current directions are marked with arrows while inactive elements are dimmed. The electric circuit diagrams correspond to their respective core diagrams by the ports marked a, b, c, d. The core diagrams include the flux rate, $\frac{d\phi}{dt} = \phi'$, induced by the inductor, as well as the flux rate induced by the transformer. The circuit operation can be understood by analysing voltage polarities and flux rates together with the right hand rule, while taking into account the switch states, current directions and diode bias.

Boost mode operation ($D_{sw} \geq 0.5$)

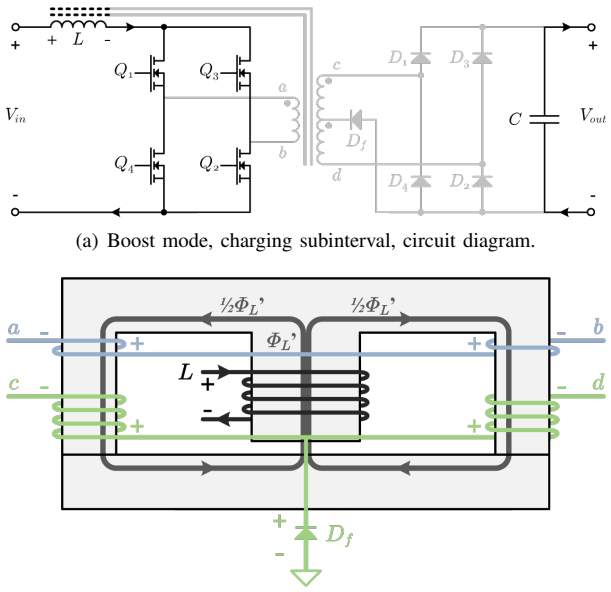
In the familiar isolated boost topology, the full-bridge switch duty cycle must be above 0.5, such that there is always a current path available for the boost inductor. This is defined as the normal boost mode operation. The gate signal is phase-shifted $180°$ between each diagonal high-side/low-side switch pair. Since $D_{sw} \geq 0.5$, the phase shifted gate signals overlap such that either all switches are on, or two diagonal switches are on.

When all switches are on, V_{in} is applied to the boost inductor, and the input current is increasing. Known as the charging or boosting subinterval, the circuit operation during this is shown in fig. 4. As seen in fig. 4(b), the flux rate induced by the inductor is uncoupled from the transformer windings due to the fact that the voltage drops induced on the transformer windings on each side leg are of opposite polarity.

The second sub-interval, referred to as the boost mode discharge subinterval, is shown in fig. 5. When two diagonal switches are on and the other two are off, the inductor current passes through the primary winding, allowing the corresponding diagonal diode pair of the output rectifier to become forward biased. The output voltage is reflected to the primary winding, such that a negative voltage drop is applied over the inductor, decreasing the current. The corresponding core diagram in fig. 5(b) shows that the inductor flux rate is decreasing, and is still uncoupled from the transformer. Additionally, it is noted that the flyback diode D_f is reverse biased.

Start-up mode operation ($D_{sw} < 0.5$)

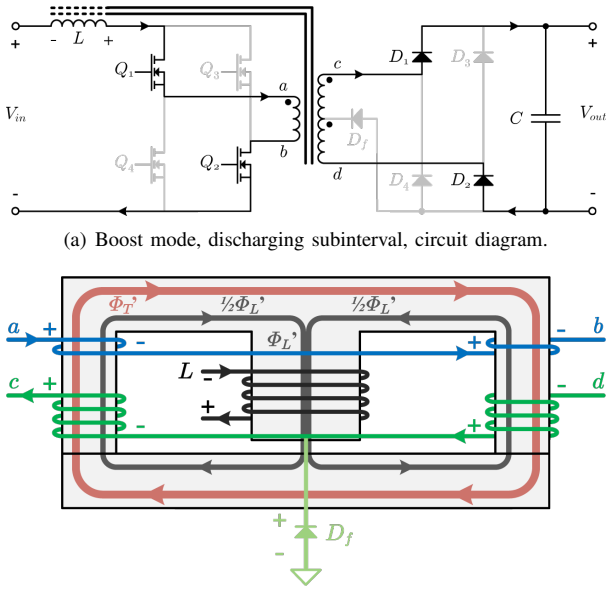
When the switch duty cycle is reduced below 0.5, the diagonal switch pairs are no longer overlapping in on-state, meaning that either two diagonal switches are on or all switches are off. When two switches are on, the circuit operation is identical to the boost mode discharge subinterval, except that the inductor current is now decreasing due to the fact that the primary voltage is lower than the input voltage, causing a positive voltage drop over L. Because of this, the subinterval is referred to as the start-up mode charging subinterval, and the corresponding circuit and core diagrams are seen in fig. 6.



(a) Boost mode, charging subinterval, circuit diagram.

(b) Boost mode, charging subinterval, core diagram.

Fig. 4. Boost mode, charging subinterval. All switches are on, inductor current is increasing. Core diagram shows that inductor flux rate is decoupled from transformer.

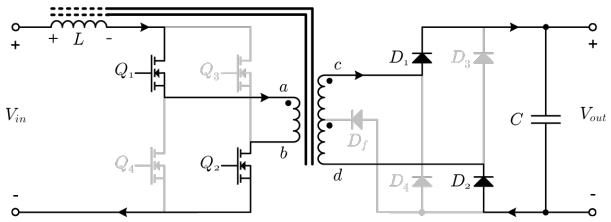


(a) Boost mode, discharging subinterval, circuit diagram.

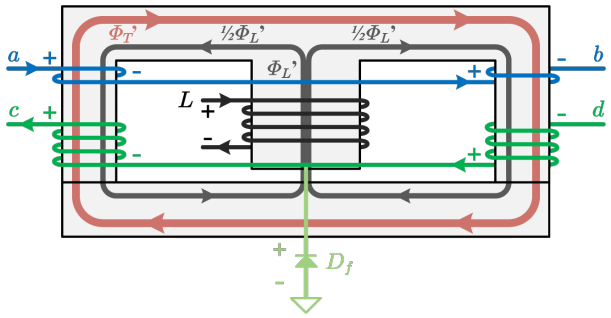
(b) Boost mode, discharging subinterval, core diagram.

Fig. 5. Boost mode, discharge subinterval. Two diagonal switches are on, inductor current is decreased by transferring energy through the transformer. It is noted that D_f is reverse biased..

When all switches are off, there needs to be an alternative current path such that the inductor flux remains continuous in order to avoid MOSFET avalanche mode clamping of the stored energy. This current path is provided by the secondary transformer winding, which thereby acts as a flyback winding during the flyback discharge subinterval seen in fig. 7. During switch turn off, the inductor current is decreasing, creating a

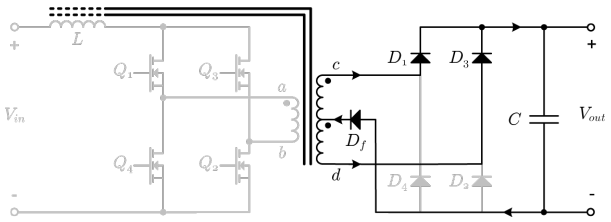


(a) Startup mode, charging subinterval, circuit diagram.

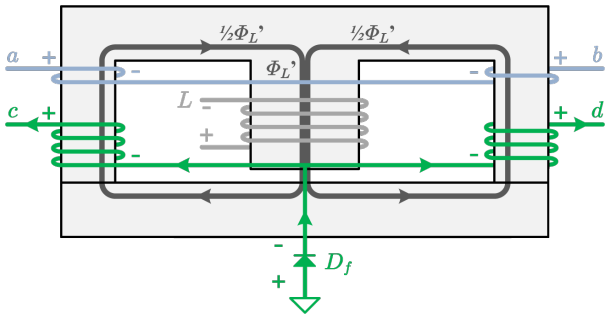


(b) Startup mode, charging subinterval, core diagram.

Fig. 6. Start-up mode, charging subinterval. Two diagonal switches are on, charging the inductor while also transferring energy through the transformer.



(a) Startup mode, discharging subinterval, circuit diagram.



(b) Startup mode, discharging subinterval, core diagram.

Fig. 7. Start-up mode, flyback discharge subinterval. All switches are turned off. The drop in inductor current causes a reverse in the associated flux rate, which couples to the secondary transformer windings. From the polarity of the induced voltages, it is evident that this allows D_f to be forward biased, such that the energy stored in the air gap can be discharged to the converter output.

reverse in the flux rate, as seen by comparing ϕ'_L on fig. 6(b) and fig. 7(b). Following the right hand rule, it is evident that this induces respective voltage drops over each half of the secondary winding, with polarities such as to allow D_f to become forward biased. The two halves of the secondary winding will then be working in parallel to discharge the energy stored in the air gap, with the full output voltage applied to each winding half.

It should be noted that it would also be possible to run the converter in "pure flyback mode", wherein either all switches are on or all switches are off. However, this means that zero energy is transferred to the output during the boosting subinterval, leading to higher current ripple at same output power. The "hybrid" startup mode shown in figs. 6 and 7 has been described in-depth as applied to a conventional external flyback winding [7], and the specific timing analysis of the previous work can be directly applied to the new integrated magnetic approach.

III. Extension to Other Isolated Boost Family Topologies

The concept can readily be applied to numerous isolated boost derived topologies, such as flyback- current-fed push-pull [8], dual inductor [9], and parallel primary isolated boost [3]. It can also be applied to various rectification circuits, including voltage doubler and center tap rectifier. Figure 8 shows the principle applied to an isolated boost converter with a center tap rectifier. In this case, the flyback diode D_f is no longer required, and the start-up functionality is gained "or free" using only the specified integrated magnetic structure, which may be beneficial in itself by reducing magnetic component count and increasing efficiency [10]. Figure 9 shows the principle applied to the parallel primary topology, which has been shown to be an efficient way of scaling isolated boost converter design for higher power [3], [4]. Additionally, the shown implementation features a shared center leg for flux cancellation, resulting in increased efficiency [11]. It is noted that only a single flyback diode is required, regardless of the degree of paralleling.

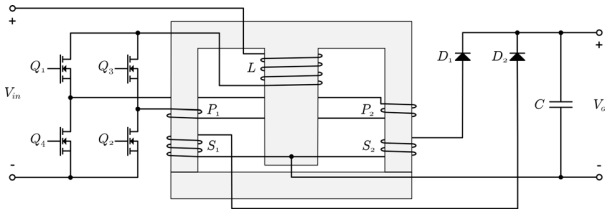


Fig. 8. New start-up method applied to isolated boost with center tap rectification circuit, where a flyback diode is not required.

Additional applications include dual inductor isolated boost and Weinberg/push-pull isolated boost topologies.

IV. Experimental Verification

An 800W isolated boost prototype as well as a 1600W parallel primary isolated boost prototype have been built in order to verify the start-up functionality, as well as to demonstrate the possibility of achieving high efficiency and high power density by application of the integration method. Both converters are hard-switched, and rely on extensive interleaving to achieve a low transformer leakage inductance

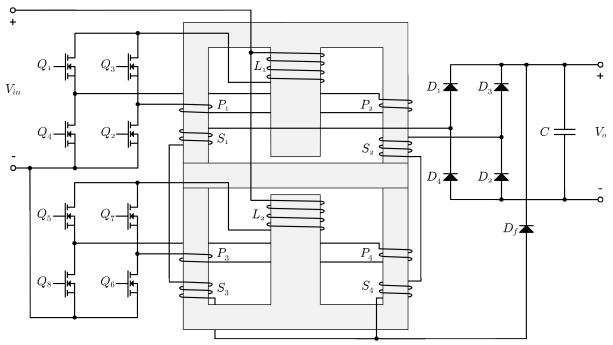


Fig. 9. New start-up method applied to parallel primary isolated boost topology.

of 91nH and 124nH respectively. The converters are designed for fuel-cell application, where a fuel cell output voltage of 25-35V is expected.

Figure 11 shows current measurements during start-up mode of the isolated boost prototype. The converter is running at $V_{in} = 25V$, $D_{sw} = 40\%$, $V_{out} = 60V$ and 100Ω load. C3 (blue) shows the AC component of the input current, C4(green) shows the AC component of the current through a high side output rectifier D_1, while C1(yellow) and C2(red) show the two gate signals.

When the gate signal C1(yellow) is high, D_1 and D_3 are forward biased, conducting a constant current through the secondary winding to the load. During this period, the boost inductor current C3(blue) is rising. After C1(yellow) goes to zero, all MOSFETs are turned off, and the boost inductor current quickly drops. At this moment, current continues flowing through D_1, safely discharging the energy stored in the boost inductor to the output. In fig. 11, C4(green) shows the current of the flyback diode D_f, clearly demonstrating the commutation of the boost inductor current.

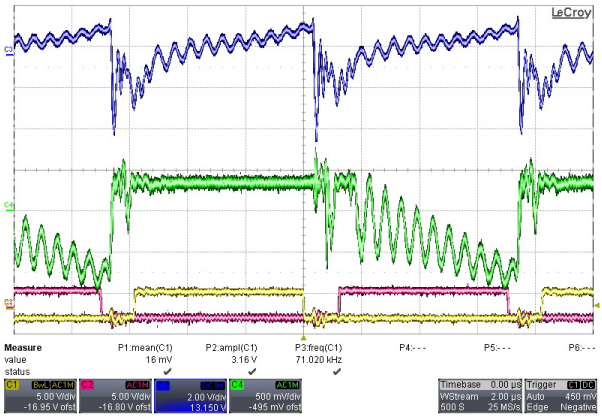


Fig. 10. Currrent waveforms of isolated boost prototype during startup mode. C3 (blue) shows the AC component of the input current, C4(green) shows the current through a high side output rectifier D_1, while C1(yellow) and C2(red) show the two gate signals.

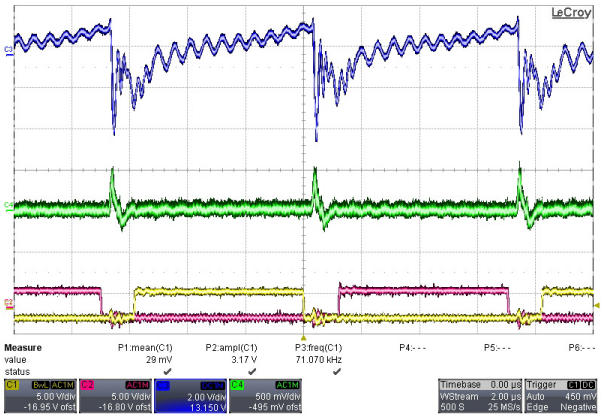


Fig. 11. Currrent waveforms of isolated boost prototype during startup mode. C3 (blue) shows the AC component of the input current, C4(green) shows the current through the flyback diode D_f, while C1(yellow) and C2(red) show the two gate signals.

A. *Efficiency Measurements*

In order to measure the efficiency during start-up of the parallel primary prototype, the duty-cycle was gradually increased from zero to 74%. A fixed load of 100Ω is used across the range, corresponding to the rated 1600W at $V_{out} = 400V$. Figure 12 shows the resulting efficiency measurements, as well as the measured output voltage at each duty cycle. The local maximum of efficiency around $D_{sw} = 20\%$ is caused by discontinuous conduction mode. Close to $D_{sw} = 50\%$, the efficiency rises dramatically, as an increasingly greater proportion of the total power is transferred through the transformer rather than the flyback operation. The converter is capable of operating continuously in start-up mode without overheating, and the voltage transitions smoothly across $D_{sw} = 50\%$.

The efficiency during normal operation was measured for both the 800W isolated boost prototype and the 1600W parallel primary. Figure 13 shows the isolated boost prototype measurements, while fig. 12 shows the results for the parallel primary prototype. Both prototypes have a peak efficiency

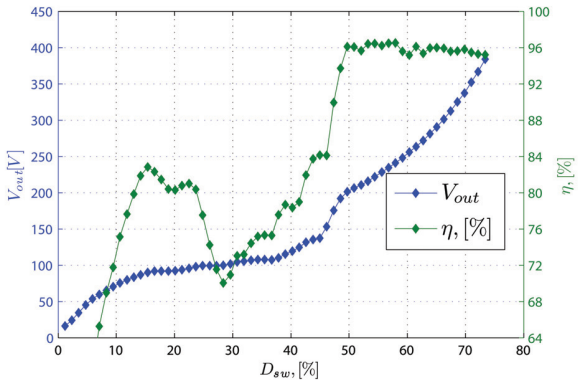


Fig. 12. Efficiency measurements of parallel primary prototype, showing efficiency and output voltage as a function of duty cycle, with a fixed load of 100Ω.

above 96% at the rated power, thus demonstrating the possibility of achieving high efficiency with the presented integration method.

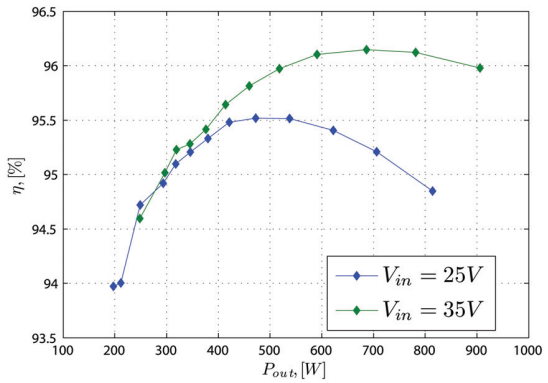


Fig. 13. Efficiency measurements of 800W isolated boost prototype, showing efficiency as a function of output power, with $V_{out} = 200V$.

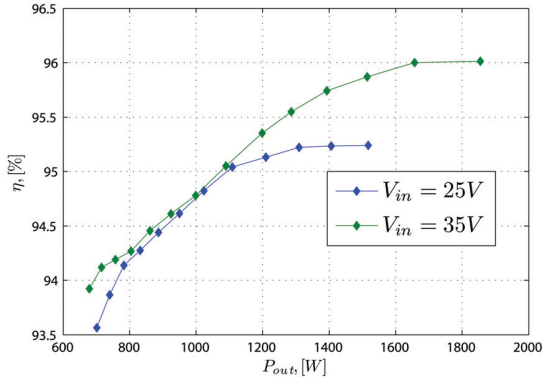


Fig. 14. Efficiency measurements of 1600W isolated boost prototype, showing efficiency as a function of output power, with $V_{out} = 400V$.

The parallel primary prototype is shown in fig. 15 and the circuit layout is visible in fig. 16, showing the underside of the converter with the heat sink removed. The parallel primary prototype uses two 6 ounce/sq.ft. copper, 8 layer PCBs, with the two fullbridges mounted directly to each primary winding to minimize stray inductance. A power density of 51 W/inch^3 was achieved, in a low profile planar layout suitable for modular configuration.

V. Conclusion

The presented start-up method effectively addresses the start-up issue of isolated boost converters, potentially paving the way for increased industry adoption of this highly promising topology family, which so far has been limited by the start-up issue. The experimental work presented has focused on fuel cell applications in the kW power range, but the method may be applied to multiple other applications. The constructed prototypes are hard-switched, and the fly-back mode is not

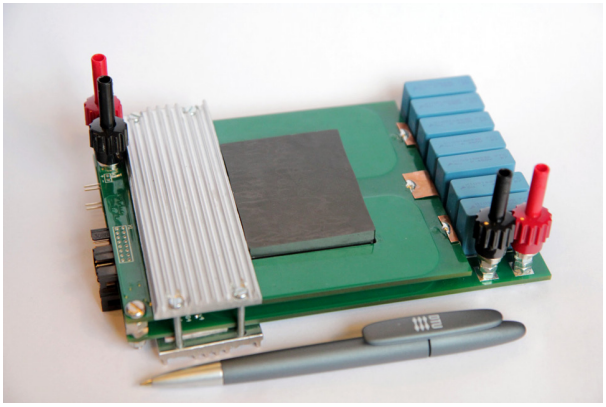


Fig. 15. Parallel primary 1600W prototype, achieving a power density of 51 W/inch^3.

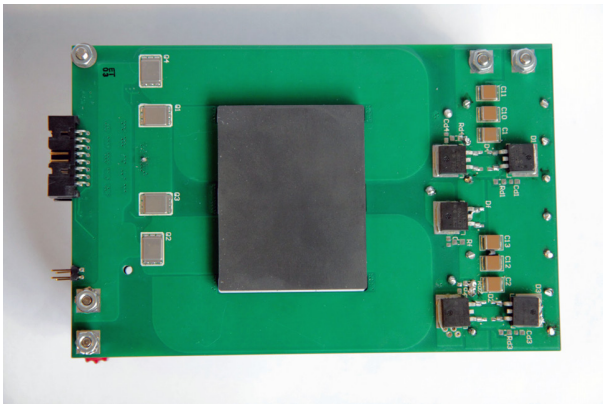


Fig. 16. Parallel primary 1600W prototype underside without heat sink. DirectFet IRF7759L2T MOSFETs are visible on the left, the ELP64 core in the middle, and C3D10060G SiC diodes including the flyback diode D_f on the right.

optimized for high efficiency but rather for fulfilling the functional requirements of start-up without affecting normal boost mode operation efficiency. Alternative applications of the method may focus on wide-range high-efficiency by employing soft-switching or regenerative snubbing, potentially making the integration method suitable for diverse applications such as Power Factor Correction and single stage inverters.

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Appendix A10

[A10] K. L.-Poulsen, Z. Ouyang, **G. Sen**, "An isolated boost flyback power converter," EU&US Patent, US application no. 61505205, and EU application no. EP11172997.6, 2011 (**Pending**).

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PATENT
059244-5PL01

U.S. PROVISIONAL PATENT APPLICATION

FOR

AN ISOLATED BOOST FLYBACK POWER CONVERTER

BY

KRISTIAN LINDBERG-POULSEN

ZIWEI OUYANG

AND

GÖKAN SEN

AN ISOLATED BOOST FLYBACK POWER CONVERTER

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FIELD OF THE PRESENT DISCLOSURE

[0002] The present invention relates to an isolated boost power converter comprising a boost inductor being wound around a first leg of a magnetically permeable multi-legged core. The boost inductor is electrically coupled between an input terminal of the boost converter and a transistor driver to be alternatingly charged and discharged with magnetic energy. A first and second series connected secondary transformer windings with a center-tap arranged in-between are wound around separate legs of the magnetically permeable multi-legged core. In a first discharge state, the magnetic energy of the boost inductor is discharged by directing a discharge current from the boost inductor through a primary transformer winding and in a second discharge state, the magnetic energy of the boost inductor is discharged by discharging a magnetic flux through the first and second secondary transformer windings. In this manner, the secondary transformer windings can replace the traditional separate flyback winding used for start-up purposes of isolated boost power converters.

BACKGROUND

[0003] Isolated boost power converters are generally accepted as a highly efficient converter topology or architecture for high power converters with low input voltage and high output voltage. Isolated boost power converters are very useful for DC-DC voltage conversion in a diverse range of applications such as fuel cell converters, electric vehicles applications and avionic applications. However, a disadvantage of prior art isolated boost power converters is the need for a so-called flyback winding during a start-up phase or state of the power converter. During start-up, a duty cycle of a Pulse Width Modulated (PWM) control signal applied to a driver circuit must be ramped-up slowly to avoid excessive in-rush currents. During ramp-up of

the duty cycle, it starts at a value much less than 0.5 which means that the driver circuit is placed in an open or cut-off state during a cycle of the PWM control signal without any low impedance path to a positive or negative input voltage terminal or rail. This situation leads to excessive voltage spikes across the boost inductor(s) which spikes may exceed the rated break-down voltage of semiconductor devices, such as MOS transistors, of the driver circuit so as to destroy these. This problem has previously been addressed by adding a flyback winding and a flyback diode to the isolated power converter providing a discharge path for energy stored in the boost inductor. However, the addition of a flyback winding has numerous drawbacks as the flyback winding is a separate power transferring element that is relatively costly, adds to size and increases component count of the boost power converter.

SUMMARY

[0004] A first aspect of the invention relates to an isolated boost power converter comprising a magnetically permeable multi-legged core. An input terminal is adapted for receipt of an input voltage, V_{in}. A boost inductor is wound around a first leg of the magnetically permeable multi-legged core where the boost inductor is electrically coupled between the input terminal and a driver to be alternatingly charged and discharged with magnetic energy. The driver has a driver output coupled to a primary transformer winding wound around a second leg of the magnetically permeable transformer core and the driver is configured to generate a primary voltage to the primary transformer winding in accordance with a driver control signal. First and second series connected secondary transformer windings with a center-tap arranged in-between are wound around separate legs of the magnetically permeable multi-legged core and a rectification circuit is coupled to respective outputs of the first and second secondary transformer windings to provide a rectified converter output voltage, V_{out}. In a first discharge state, the magnetic energy stored in the boost inductor is discharged by directing a discharge current from the boost inductor through the primary transformer winding. In a second discharge state, the magnetic energy stored in the boost inductor is discharged by discharging a magnetic flux through the first and second secondary transformer windings.

[0005] The ability provided by the present isolated boost power converter to discharge magnetic energy stored in the boost inductor through the first and second secondary transformer windings provides a novel solution to start-up of isolated boost power converters/DC-DC

converters allowing these to operate below 50% duty cycle, D, of a Pulse Width Modulated (PWM) driver control signal. Consequently, the output voltage range at V_{out} can be extended down to zero without use of the traditional separate flyback winding as the first and second secondary transformer windings provide the functionality of the separate flyback winding of prior art boost power converters. The omission of the traditional separate flyback winding leads to a significant simplification of electric and magnetic circuit design, reduces component count, improves reliability, reduces the price and size of the power converter and decreases manufacturing costs. Furthermore, power conversion efficiency during start-up, and generally operation below 50% duty cycle of the PWM driver control signal, is improved without affecting normal boost operation because copper material is not wasted on the traditional flyback winding. It is also noticeable that secondary transformer winding normally is designed for low winding resistance such that the flyback winding functionality requires no modification of an existing secondary transformer winding. The normal low resistance of existing secondary transformer windings also means that its use as flyback winding in accordance with the present invention can increase power efficiency compared with the traditional separate flyback winding. Furthermore, the second discharge state also allows stored magnetic energy in the boost inductor to be discharged or dissipated during error states of the isolated boost converter which e.g. may arise in case of switching errors in the driver or an output short circuit condition.

[0006] The skilled person will understand that the term “isolated” does not imply that the input and output sides of the present isolated boost power converter necessarily are galvanically isolated by the magnetically permeable multi-legged core even though they may be so in some embodiments of the invention. Respective negative terminals or rails of the rectified output voltage V_{out} and the input voltage V_{in} may be electrically coupled to each other, for example through a shared GND connection such that a galvanic connection is established between the input/primary and output/secondary sides of the isolated boost power converter.

[0007] According to a preferred embodiment, during the second discharge state the first and second secondary transformer windings are coupled in parallel from the center-tap arranged between first and second series connected secondary transformer windings to the rectified converter output voltage, V_{out}. This allows discharge current to be directed to the rectified converter output voltage by both half-windings so as to minimize conductive losses in the

secondary transformer winding. The magnetic flux flowing through the first and second secondary transformer windings, generated by the magnetic energy stored in the boost inductor, is converted to respective discharge currents flowing through the first and second secondary half windings SW_1 and SW_2. Thereby, power or energy is transferred to the rectified converter output voltage so as to control the latter when the output voltage is below a minimum voltage required for normal boost mode operation.

[0008] The present isolated boost converter is preferably configured such that the second discharge state is automatically entered when the driver enters a non-conducting or OFF-state for example when a duty cycle of a pulse width modulated driver control signal is less than 0.5. The driver may for example enter the non-conducting state when all transistors of the driver simultaneously are in non-conducting states. The driver may comprise a half-bridge or an H-bridge with two or four MOS transistors, respectively. The H-bridge or full-bridge transistor driver may have first and second complementary driver outputs coupled to respective ends of the primary transformer winding. When all transistors of the half-bridge or full-bridge transistor driver are placed in non-conducting states by the pulse width modulated driver control signal, a voltage across the driver rapidly rises to a destructive level due the continued effort of the boost inductor to transmit current towards the driver. This undesired rise of boost inductor voltage takes place during start-up of the isolated boost converter where the duty cycle D of the pulse width modulated driver control signal must be initialized to a value below 0.5, preferably close to zero, to avoid large in-rush currents. However, the automatic entry into the second discharge state provided by this embodiment eliminates the generation of destructive boost inductor voltage spikes by discharging the magnetic energy stored in the boost inductor as the discharge currents running through the first and second secondary transformer windings. The automatic entry of the second discharge state may be caused by a reverse in a flux rate through the boost inductor due to a sudden decrease of boost inductor current.

[0009] In accordance with a preferred embodiment of the invention, the boost converter is configured to change between the first and second discharge states by selectively coupling and decoupling the boost inductor from the secondary transformer windings such that:

- during the first discharge state, magnetically decoupling the boost inductor from the first and second secondary transformer windings to deliver the magnetic energy to the primary transformer winding;

- during the second discharge state, magnetically coupling the boost inductor to the first and second secondary transformer windings through a shared flux path in the magnetically permeable multi-legged core. The shared flux path may comprise two separate shared flux paths such that a first shared flux path runs between the boost inductor and the first secondary transformer winding and a second shared flux path runs between the boost inductor and the second secondary transformer winding. The number of windings of the first and second secondary transformer windings is preferably substantially identical to allow effective decupling between the boost inductor and the first and second secondary transformer windings in the first discharge state.

[0010] As previously mentioned the first and second secondary transformer windings are preferably configured to discharge the magnetic energy stored in the boost inductor by supplying a discharge current to the rectified converter output voltage, V_{out}, so as to transfer energy to the output. In this scheme the first and second secondary transformer windings act as a flyback winding.

[0011] According to an advantageous embodiment of the invention, the magnetically permeable multi-legged core comprises:

- a center leg, having an air gap arranged therein,
- a first outer leg and a second outer leg; The boost inductor is magnetically coupled to the center leg to store the magnetic energy therein and the first and second secondary transformer windings are wound around the first and second outer legs, respectively. This topology of the magnetically permeable multi-legged core may comprise a conventional EI core. The air gap is well-suited for storage of the magnetic energy due to its high reluctance or low magnetic permeability and preferably has a height between 0.1 mm and 10 mm. In one embodiment, the boost inductor is wound around the center leg while in other embodiments windings of the boost inductor is split into two series connected half-windings wound around respective ones of the first and second outer legs. In the latter embodiment, the boost inductor is magnetically coupled to the air gap by a suitable magnetically permeable structure of the magnetically permeable multi-legged core.

[0012] In yet another embodiment of the invention which comprises the center leg with the air gap and the first and second outer legs, the primary transformer winding comprises first and second series connected half-windings wound around the first and second outer legs, respectively, of the magnetically permeable multi-legged core. In this embodiment, the first half-winding of the primary transformer winding and the first secondary transformer winding are both

wound around the first outer leg of the magnetically permeable multi-legged core. Likewise, the second half-winding of the primary transformer winding and the second secondary transformer winding are both wound around the second outer leg of the magnetically permeable multi-legged core.

[0013] The skilled person will understand that the present isolated boost power converter may comprise many different types of primary side circuit topologies in addition to the previously mentioned half-bridge and full-bridge drivers. In one embodiment, the primary side comprises a first boost inductor and a second boost inductor such that the first boost inductor is coupled between the input terminal and a first transistor driver output. The first transistor driver output is coupled to a first end or first winding output of the primary transformer winding. The second boost inductor is coupled between the input terminal and a second transistor driver output. The second transistor driver output is coupled to a second end or second winding output of the primary transformer winding. The first and second transistor driver outputs may comprise respective drain or collector terminals of a MOS or bipolar transistor. The use of at least two boost inductors is advantageous because this reduces driver component count such as reducing the number of switch transistors.

[0014] In another embodiment, the boost inductor comprises a first half-winding and a second half-winding of the primary transformer winding to provide an integrally formed boost inductor and primary winding which is advantageous because of improved copper utilization. In this embodiment, the magnetic energy stored in the boost inductor is directly transferred to the first and second secondary transformer windings by a magnetic flux through the magnetically permeable multi-legged core. In the above-discussed embodiments with separate primary transformer winding and boost inductor, magnetic energy is initially stored in the boost inductor and subsequently released or discharged, during the first discharge state, as discharge current flowing through the primary transformer winding to induce a primary side voltage therein.

[0015] In a number of embodiments of the isolated boost power converter a rectifying element is electrically coupled to the center-tap to conduct a discharge current, during the second discharge state, from the first and second secondary transformer windings to the rectified converter output voltage, V_{out}. The discharge current is induced by the magnetic flux generated by the boost inductor flowing through the first and second secondary transformer windings. The rectifying element is preferably electrically coupled to a supply rail, such as ground, a negative

supply rail or a positive supply rail, of the secondary side of the isolated boost power converter. The rectifying element may be required if the rectification circuit comprises a full-bridge rectifier or a voltage doubler because during the first discharge state, the center-tap voltage is different from both the rectified converter output voltage and a negative rectified converter output voltage.

[0016] Alternatively, the rectification circuit may comprise a center-tapped rectifier in accordance with a preferred embodiment of the invention where a rectifying element coupled in series with the center-tap can be avoided. According to this embodiment, the center-tap is electrically connected to a negative rectified converter output voltage or the rectified converter output voltage, V_{out},

- the respective outputs of the first and second secondary transformer windings are coupled to the opposite output voltage to the one electrically coupled to the center-tap through first and second rectifying elements. Each of the first and second rectifying elements preferably comprises a semiconductor diode.

[0017] As previously mentioned, the rectification circuit may comprise a voltage multiplier for example a voltage doubler circuit to increase the level of the rectified converter output voltage, V_{out}. The skilled person will understand that the rectifying element and/or the rectification circuit each may comprise one or more semiconductor diode(s), diode-coupled transistor(s) or synchronously controlled transistor switch(es). Each of the semiconductor diodes may comprise a MOS diode, a bipolar diode, a Schottky diode or any combination thereof.

[0018] According to one advantageous embodiment or variant of the invention discussed above with the center leg surrounded by the first and second outer legs, the isolated boost power converter comprises:

- a second magnetically permeable multi-legged core and a second boost inductor magnetically coupled to a center leg of the second magnetically permeable multi-legged core to store magnetic energy therein. The second boost inductor being electrically coupled between the input terminal and a second driver to be alternatingly charged and discharged with magnetic energy. The second driver having a second driver output coupled to a second primary transformer winding wound around a first outer leg and a second outer leg of the second magnetically permeable transformer core. The second driver is configured to generate a second primary voltage to the

second primary transformer winding in accordance with the driver control signal. The boost power converter further comprises first and second secondary transformer windings wound around the first outer leg and the second outer leg, respectively, of the second magnetically permeable multi-legged core. The first secondary transformer winding of the second magnetically permeable multi-legged core is coupled in series between the rectification circuit and the output of the first secondary transformer winding of the first magnetically permeable multi-legged core. The second secondary transformer winding of the second magnetically permeable multi-legged core is coupled in series between the rectification circuit and the output of the second secondary transformer winding of the magnetically permeable multi-legged core, or first magnetically permeable multi-legged core, such that:

- in the first discharge state, the respective magnetic energies stored in the first and second boost inductors are discharged by directing respective discharge currents from the respective boost inductors through the respective primary transformer windings,
- in the second discharge state, the respective magnetic energies stored in the respective boost inductors are discharged by discharging respective magnetic fluxes through the respective first and second secondary transformer windings.

[0019] According to the latter embodiment of the invention, the first and second secondary transformer windings of the first magnetically permeable multi-legged core are electrically coupled to the rectification circuit in an indirect manner through the respective ones of the first and second secondary transformer windings of the second magnetically permeable multi-legged core. The first and second secondary transformer windings are therefore coupled in series such that the rectified converter output voltage, V_{out} is doubled in a symmetrical architecture or topology of transformer windings on the first and second magnetically permeable multi-legged cores. The first and second magnetically permeable multi-legged cores may be provided as separate parts, for example arranged in abutment or proximate to each other, or as an integrally formed element which has a common magnetically permeable structure or leg. In a preferred embodiment, the first and second magnetically permeable multi-legged cores share a common magnetic flux path extending through a shared magnetically permeable leg. In the latter embodiment, the first and second magnetically permeable multi-legged cores may advantageously be configured to provide magnetic flux cancellation or suppression in the shared magnetically permeable leg. This saves magnetic material such that material costs and size of the

isolated boost power converter is reduced. The above-discussed embodiments of the present invention based on the first and second magnetically permeable multi-legged cores possess numerous favourable characteristics: These embodiments are readily scalable by the addition of further magnetically permeable multi-legged cores, associated primary side and secondary side transformer windings and drivers. This property means that isolated boost power converters can readily be adapted to a whole range of applications with varying power capacity. Thus, saving design time, reducing design risk and reducing manufacturing costs etc. In addition, the current rating of each semiconductor switch of the first and second drivers can be halved for a given current handling capacity due to the split of input current between the first, second and possibly further drivers.

[0020] The driver control signal may comprise a PWM signal having an adjustable duty cycle, D. The adjustable duty cycle may be used to set a desired or target DC level of the rectified converter output voltage, V_{out}. The duty cycle is preferably set to a value between 0.5 and 1.0 after exiting from a start-up state or mode, i.e. during normal boost mode operation of the isolated boost converter. The duty cycle, D, may be set or controlled in connection with a closed loop control scheme for controlling any of the state variables of the isolated power converter, such as the boost inductor current or the rectified converter output voltage, $V_{out.}$

[0021] Another aspect of the invention relates to a method of generating a rectified converter output voltage, V_{out}, from an input voltage, V_{in}, by an isolated boost power converter according to any of the preceding claims. The method comprises steps of:

- generating a pulse width modulated driver control signal,
- supplying the pulse width modulated driver control signal to the driver,
- gradually increasing a duty cycle, D, of the pulse width modulated driver control signal from below 0.5, preferably below 0.1, to a value above 0.5, preferably between 0.55 and 0.99,
- adjusting the duty cycle, D, to a desired value to reach a desired or target AC voltage waveform or DC voltage level at the rectified converter output voltage, $V_{out.}$. As previously explained, before the isolated boost converter reaches its normal operating state, a start-up mode or state is required. During the start-up phase or mode of the isolated boost power converter the duty cycle of the Pulse Width Modulated (PWM) driver control signal applied to the driver must be ramped-up slowly to avoid excessive in-rush currents. During ramp-up of the duty cycle, it

preferably starts at a value much less than 0.5 which means that the driver is placed in an open or cut-off state during a certain time interval of a cycle of the PWM signal. The open state of the driver means the driver lacks a low resistive path to the input voltage or a negative input voltage rail such as ground, GND. However, thanks to the ability of the first and second secondary transformer windings to discharge the magnetic flux stored in the boost inductor, the present isolated boost power converter can enter and exit the start-up mode so as to establish an initial output voltage as V_{out} without any need for a separate flyback winding or other auxiliary start-up circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] A preferred embodiment of the invention will be described in more detail in connection with the appended drawings, in which:

[0023] Figs. 1a) and 1b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, of an isolated boost power converter in accordance with a first embodiment of the invention,

[0024] Figs. 2a) and 2b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, of the isolated boost power converter in accordance with the first embodiment of the invention during a charging subinterval of boost mode operation,

[0025] Figs. 3a) and 3b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, of the isolated boost power converter in accordance with the first embodiment of the invention during a first discharge state of the boost mode operation,

[0026] Figs. 4a) and 4b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, of the isolated boost power converter in accordance with the first embodiment of the invention during a charging subinterval of a start-up mode.

[0027] Figs. 5a) and 5b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, of the isolated boost power converter in accordance with the first embodiment of the invention during a second discharge state of the start-up mode wherein magnetic energy stored in a boost inductor is discharged by discharging a magnetic flux through secondary transformer windings,

[0028] Fig. 6a) is an electrical circuit diagram of an isolated boost power converter with integration of a boost inductor and primary transformer windings in accordance with a second embodiment of the invention,

[0029] Fig. 6b) is an electrical circuit diagram of an isolated boost power converter with a center-tapped rectification circuit in accordance with a third embodiment of the invention,

[0030] Fig. 7 is an electrical circuit diagram of an isolated boost power converter with an integrally formed dual core topology in accordance with a fourth embodiment of the invention; and

[0031] Fig. 8 is a graph depicting measurement data from an experimental isolated boost power converter in accordance with the first embodiment of the invention.

DETAILED DESCRIPTION

[0032] The embodiments described in detail below are particularly well-suited for power converters providing DC voltage amplification or step-up. However, the skilled person will understand that power converter in accordance with the present invention are highly useful for other types of applications both in step-up and step down voltage converting applications.

[0033] Fig. 1a) illustrates schematically an electrical circuit diagram of an isolated boost power converter 100 in accordance with a first embodiment of the present invention. The isolated boost power converter 100 comprises a magnetically permeable multi-legged core in form of the three legged EI core 102. The three legged EI core 102 comprises a center leg 134 surrounded by a first outer leg 132 and a second outer leg 136 in a mirror-symmetrical layout or structure about a central vertical axis extending through the center leg 134. The center leg 134 comprises an air gap 138 which allows magnetic energy of a boost inductor, L_{boost}, to be stored therein. The isolated boost power converter 100 comprises an input terminal 104 for receipt of an input voltage, Vin, which for example may be a DC voltage between 5 Volt and 100 Volt. The boost inductor, L_{boost}, is arranged or wound around a first leg of the three legged EI core 102 and electrically coupled between the input terminal 104 and a transistor driver 106 to be alternatingly charged and discharged with magnetic energy through the transistor driver 106. The primary and secondary windings are both split into two half-windings distributed between the first and second EI core legs so that the flux from the boost inductor, L_{boost}, is decoupled from

the transformer function in normal boost operation. The transformer winding outputs or ports are marked a; b; c and d in both the electrical circuit diagram of Fig. 1a) and the magnetic diagram of Fig. 1b). The transistor driver 106 comprises four NMOS transistors $S_1 - S_4$ coupled as a full-bridge or H-bridge such that a first driver output, at a shared junction or node in-between the NMOS transistors S_1 and S_4, is electrically coupled to the first winding output, a, of a primary transformer winding or primary side transformer winding PW_{1-2}. A second driver output, at a shared junction or node in-between NMOS transistors S_2 and S_3, is electrically coupled to the second winding output, b, of the primary transformer winding PW_{1-2}. The primary transformer winding PW_{1-2} is split as mentioned above so as to comprise two series connected half-windings PW_1 and PW_2 (refer to Fig. 1b)) wound around the first and second outer legs, 132, 136, respectively, of the EI core 102.

[0034] The transistor driver 106 consequently generates a primary voltage across the primary winding 110 in accordance with a driver control signal, such as a pulse width modulated control signal, adapted to individually control the switching of the NMOS transistors S_1 - S_4, which each are switched between conducting and non-conducting states, i.e. On or Off. The isolated boost power converter 100 comprises first and second series connected secondary transformer windings, SW_1 and SW_2, respectively, having a center-tap or midpoint 116 arranged in-between them. The first and second series connected secondary transformer windings, SW_1 and SW_2, respectively, are wound around the first outer leg 132 and the second outer leg 136, respectively, i.e. separate legs of the EI core 102 such that the second secondary transformer winding SW_2 is arranged on the same outer leg 136 as the half-winding PW_2 of the primary transformer winding and the first secondary transformer winding SW_1 is arranged on the same outer leg 132 as the half-winding PW_1 of the primary transformer winding. A voltage transfer ratio between the primary and secondary sides of the transformer function provided by the EI core 102 is set by a turns ratio, *n*, between a number of secondary side transformer windings relative to a number of primary side transformer windings. In the present embodiment, this turns ratio, *n*, equals the

number of secondary transformer windings of SW_1 and SW_2 combined divided by the number of primary transformer windings of PW_1 and PW_2 combined. The turns ratio, *n*, may naturally vary with requirements of a particular application, in particular whether the boost converter is intended to function as a step-up or step-down converter. The turns ratio, *n*, is preferably set to value between 0.25 and 100 such as between 1.0 and 64. The integration on the common or shared EI core 102 of the boost inductor, L_{boost}, the primary transformer winding PW_{1-2} and the first and second series connected secondary transformer windings, SW_1 and SW_2 is often referred to as ”integrated magnetics” in the art.

[0035] A rectification circuit 118 is electrically coupled to respective outputs of the first and second secondary windings to provide a rectified converter output voltage, V_{out}, between rectified converter output voltage, V_{out}, 119 and a negative rectified converter output voltage 121. A supply capacitor C or C_{out} is coupled between these converter output voltages or rails to suppress ripple voltages at the output of the rectification circuit 118 and provide an energy reservoir stabilising the output voltage, V_{out}. In the depicted isolated boost power converter 100, the input side or primary side and secondary side are galvanically isolated by the EI core 102. However, the skilled person will understand that the negative terminals or rails of the output voltage V_{out} and the input voltage may be electrically coupled to each other, for example through a shared GND connection without compromising the desired boost inductor discharge functionality of the first and second secondary transformer windings of the present isolated boost power converter 100. A rectifying element in form of a semiconductor diode, D_f, is coupled between the center-tap 116 and the negative rectified converter output voltage 121 to facilitate a flow of discharge current through the first and second secondary transformer windings, SW_1 and SW_2, respectively. The discharge current subsequently flows through the rectification circuit 118 and to the output terminal or node 119 providing the rectified converter output voltage, V_{out}, so as to transfer energy to the output, facilitating start-up of the power converter 100 as explained in further detail below.

[0036] The transfer characteristic of the isolated boost converter is set by a duty cycle, D, of the Pulse Width Modulated (PWM) driver control signal, during normal boost operation according to:

$$\frac{V_{out}}{V_{in}} = \frac{n}{2(1-D)} \Leftrightarrow V_{out} \geq \frac{nV_{in}}{2}$$

(Equation 1) wherein:

V_{out} = rectified DC output voltage of the boost converter,

V_{in} = the DC input voltage to the boost converter;

D = a duty cycle of the PWM control signal at each transistor input of the driver and defined as: T_{on}/T_{period} of a single PWM period;

n = transformer turns ratio set by the number of secondary transformer windings divided by the number of primary transformer windings.

[0037] When $V_{out} \leq \frac{nV_{in}}{2}$, the isolated boost converter may be in the start-up phase and the duty cycle, D, of the Pulse Width Modulated (PWM) driver control signal below 0.5.

[0038] Fig. 2a) illustrates schematically an electrical circuit diagram 100 of the isolated boost power converter during a first subinterval or state boost mode operation. Circuit elements that are not carrying current have been dimmed to clarify the operation during the first state. Generally, when the duty cycle of the driver control signal, D, exceeds 0.5, the isolated boost power converter 100 operates as a normal isolated boost converter. The boost mode operation can be divided into two subintervals: The first state or boosting subinterval where all the NMOS transistors S_1-S_4 are in placed in respective conducting states or on states. A second state of the boost mode operation is an energy transfer subinterval where two of the NMOS transistors, either S_1-S_2 or S_3-S_4 , are in conduction states simultaneously as illustrated on Fig. 3a) and Fig. 4a). In the latter state or subinterval boost inductor current is allowed to flow through the primary transformer winding $PW_{1\text{-}2}$ such that energy or power is transferred through the EI core 102 to the rectified output voltage. The positive direction of any currents is indicated by arrows on electrical conductors or wires and relevant voltage polarities indicated by +/- signs. Fig. 2b) shows the magnetic diagram, including flux rate induced by the boost inductor winding: $d\Phi/dt = \Phi_{L'}$, shown by fat dotted lines 112a and 112b. The rising current in L_{boost} corresponds to a

positive voltage drop of the input voltage, $V_{in.}$ The DC flux is excluded from the analysis and the illustrated drawing as this is only relevant for magnetic saturation and power loss considerations of the EI core 102. The induced magnetic flux Φ_L, splits evenly between the first and second outer legs 132, 136, respectively, inducing voltage drops on the transformer windings with polarities indicated by the indicated +/- signs at respective winding outputs a, b, c and d following from the right hand rule. The polarities across the two series connected primary side half-windings PW_1, PW_2 are opposite, and the voltages cancel and likewise for induced voltages across the two series connected secondary side half-windings SW1 and SW2, so it can be concluded that the boost inductor L_{boost} or L is not coupled to the transformer function of the EI core 102 during this state or subinterval. Furthermore, it is also evident that D_f is reverse biased in the illustrated subinterval of boost mode operation.

[0039] Fig 3a) illustrates schematically the electrical circuit diagram of the isolated boost power converter 100 during a first discharge state, or transformer energy transfer subinterval, of the boost mode. Circuit elements that are not carrying current have been dimmed to clarify the operation in this state. During the illustrated energy transfer subinterval, the two series connected primary side half-windings PW_1, PW_2 or primary winding PW_{1-2} of the EI core based transformer is connected in series with the boost inductor, such that the magnetic energy stored in the boost inductor is discharged by a discharge current flowing through the primary transformer winding such that energy is transferred to the rectified output voltage. The current direction through the primary winding PW_{1-2} is alternated for every other subinterval, such that either NMOS transistors S_1; S_2 and rectifying diodes D_1 and D_2 or NMOS transistors S_3, S_4 and rectifying diodes D_3 and D_4 are conducting . Fig.3a) shows the subinterval where the NMOS transistors S_1, S_2 and rectifying diodes D_1 and D_2 are conducting.

[0040] Fig. 3b) shows the magnetic diagram, including a flux rate, $d\Phi/dt = \Phi_L$', induced by the boost inductor L_{boost}. A first flux path associated with the boost inductor extends around the center leg 134, the first outer leg 132 and the air gap 138 as illustrated symbolically by fat dotted line 112a. Likewise, a second flux path extending around the center leg 134, the second outer leg

132 and the air gap 138 is illustrated symbolically by fat dotted line 112b. The flux rate induced by the primary winding $PW_{1-2,}$ $d\Phi_T/dt = \Phi_T'$, is shown by an outer fat dotted line 114 illustrating how the flux circulates clockwise around an outer closed path or loop 114 around the outer periphery of the EI core 102 including the first and second outer legs 132, 136, respectively. As seen in Fig.3b), the flux rate Φ_T' flows in a low reluctance outer path of the EI core 102 avoiding to travel across the air gap 138 due to its high reluctance or low magnetic permeability. Using the right hand rule and the depicted voltage polarity on the two half-windings PW_1, PW_2 of the primary winding, it can be seen that these two flux rates are in the same direction along the outer flux path depicted by the fat dotted line 114. In the same manner, it is evident that the flux rate Φ_T' couples to the secondary side half-windings SW_1 and SW_2 such that induced current flows from winding output d to the winding output c, forward biasing the rectifying diodes D1 and D2. From this it follows that output voltage at the mid-point 116 between the secondary side half-windings is positive with approximately one-half of the rectified converter output voltage, V_{out}, such that D_f is reverse biased.

[0041] When instead NMOS transistors S_3, S_4 and rectifying diodes D_3 and D_4 are conducting, a corresponding analysis applies due to symmetry. In the latter case, all transformer winding voltages and currents are reversed, which still results in D_f being reverse biased by one-half of V_{out}. It is also worthwhile to notice that in both cases, the flux rate induced by the boost inductor, L, is not coupling to the primary and secondary transformer windings PW_{1-2}, and $SW_{1,}$ SW_2, respectively, of the EI core 102 such that the boost inductor is magnetically decoupled from the transformer operation. Furthermore, the current in the boost inductor, L, is falling, seen as a negative voltage drop across the boost inductor in both Figs. 3a) and b).

[0042] Figs. 4a) and b) show schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, during a charging subinterval of a start-up mode. The input voltage, Vin is charging the boost inductor while also transferring energy to the rectified output voltage through the transformer operation of the EI core 102 of the isolated boost power converter 100. This charging subinterval can be viewed as a hybrid boost and energy transfer subinterval. The MOS transistors S_1, S_2 of the driver 106 and rectifying diodes D_1 and D_2 are

conducting. The operation is identical to the second subinterval discussed above in connection with Figs. 3a) and 3b) except current in the boost inductor, L, or L_{boost} is increasing as indicated by the reversed polarity of the voltage across the boost inductor. The term "hybrid" indicates that the boost inductor, L, and the primary transformer winding, PW_{1-2}, are both active such that magnetic energy is loaded into the boost inductor, L, at the same time as energy is transferred to the rectified output voltage through the transformer operation between the primary and secondary windings PW_{1-2}, and SW_1, SW_2, respectively, of the EI core 102. Consequently, during the first discharge state, the flux rate Φ_L, induced by the boost inductor, L, is decoupled from the secondary transformer windings SW_1, SW_2 of the EI core 102 such that the boost inductor is substantially magnetically decoupled from the transformer operation.

[0043] Figs. 5a) and 5b) illustrate schematically an electrical circuit diagram and a magnetic circuit diagram, respectively, the isolated boost power converter 100 during a second discharge state. Magnetic energy stored in a boost inductor, L, is discharged by discharging a magnetic flux through secondary transformer windings SW_1, SW_2. Circuit elements that are not carrying current have been dimmed to clarify the operation during the second discharge state of start-up mode.

[0044] During the second discharge state, which can be viewed as a second subinterval of the start-up mode, the magnetic energy stored in the boost inductor, L, is discharged by circulating the stored magnetic flux through the first and second secondary transformer windings SW_1, SW_2. When all the NMOS transistors S_1 - S_4 of the driver circuit 106 are turned off, i.e. non-conducting, the boost inductor current commutates to the first and second secondary transformer windings SW_1, SW_2 through the flyback diode D_f, as shown in Fig. 5a) by a magnetic coupling 108 as symbolically indicated on Fig. 5a). A shared magnetic flux path comprising the first and second flux paths 112a, 112b (refer to Fig. 5b)) extending around the first and second outer legs, 132, 136, respectively, magnetically coupling the boost inductor, L, to the first and second secondary transformer windings SW_1, SW_2. The cutoff or non-conducting state of the NMOS transistors of the driver leads to a suddenly dropping boost inductor current which results in a reverse in the respective rates of fluxes $\frac{1}{2}\Phi_L$, at the first and second flux paths 112a, 112b

whereby the voltage polarity across the boost inductor is reversed (compared to Fig. 4b)). This flux rate reversal of $\frac{1}{2}\Phi_L$, induces a voltage drop across each of the secondary side half-windings SW_1 and SW_2. There is a positive voltage drop from secondary winding output c to D_f as well as from secondary winding output d to rectifying diode D_f. Consequently, a discharge current, I_d, can now travel from secondary winding output c through D_1 and into the load resistance R_L continuing back through D_f. Similarly, a discharge current can travel from secondary winding output d through D_3 into R_L and back through D_f. In effect, during the second discharge state of the start-up mode, the two secondary half windings SW_1 and SW_2 are working or coupled electrically in parallel from the center-tap 116 to the rectified output voltage V_{out} through respective rectifying diodes D_1 and D_2 so as to jointly discharge the magnetic energy in the boost inductor. This magnetic energy is largely stored in the air gap 138. As illustrated, the magnetic energy stored in the boost inductor is converted to discharge currents flowing through the first and second secondary half windings SW_1 and SW_2 to the rectified converter output voltage, V_{out} through the shared magnetic flux path 112a, 112b. Consequently, the the boost inductor, L, is magnetically coupled to the first and second secondary transformer windings SW_1 and SW_2. In effect, transferring energy to the rectified output voltage during the start-up mode and allowing a gradual transition towards a state of normal boost mode operation for the isolated boost power converter 100.

[0045] Fig. 6a) is an electrical circuit diagram of an isolated boost power converter 600 in accordance with a second embodiment of the invention. The isolated boost power converter 600 is similar to the previously described isolated boost converter 100 except for the reversal of the polarity of the rectifying diode D_f and an accompanying reversal of a winding orientation of the boost inductor L_{boost} relative to the winding orientation depicted on Fig. 1b). Like features have been marked with corresponding numerals to assist the comparison. The skilled person will notice that this configuration of the rectifying diode D_f works similarly to the above-described

configuration, in that when the primary transformer winding is inactive, a decreasing flux in the center leg will cause D_f to be forward biased in either case.

[0046] Fig. 6b) is an electrical circuit diagram 640 of an isolated boost power converter with a center-tapped rectification circuit 648 in accordance with a third embodiment of the invention. The transistor based full-bridge driver 606, the primary and secondary windings PW_1, PW_2 and SW_1, SW_2, respectively, and the EI core 102 itself are preferably all identical to the same features of the above-discussed first embodiment of the present isolated power converter. However, in the present embodiment, the rectification circuit only comprises two rectifying diodes D_1 and D_2 coupled from a first winding output of the first half-winding SW_1 and second winding output of the second half-winding SW_2, respectively, to a rectified converter output voltage, V_{out}, at positive and negative output nodes 619, 621, respectively. However, as a center-tap voltage at node 616 arranged in-between the first and second secondary transformer half-winding SW_1, SW_2 is always held at the negative rectified converter output voltage on output node 621, which may be ground level GND, there is not any need to add a rectifying diode D_f in series with the center-tap 616 like in the previously discussed embodiments.

[0047] Fig. 7 is an electrical circuit diagram of an isolated boost power converter 700 with a dual core topology comprising an integrally formed multi-legged EI core 702a, 702b in accordance with a fourth embodiment of the invention. The isolated boost power converter 700 comprises an integrally formed magnetically permeable multi-legged core in form of a first three legged EI core 702a and a second three legged EI core 702b that share a common "I" leg 740 such that the entire magnetically permeable multi-legged core is a unitary structure. The structure of the integral magnetically permeable multi-legged core 702a, 702b is mirror symmetrical about a horizontal symmetry axis 750. Each of the EI cores 702a, 702b comprises a center leg 734a, 734b, respectively, surrounded by a first outer leg 732a,b and a second outer leg 736a,b in a mirror-symmetrical layout or structure about a central vertical axis extending through a middle of the center legs 734a, 734b.

[0048] Each of the center legs 734a, 734b comprises an air gap 738a, 738b which allows magnetic energy of an associated boost inductor, L_{boosta}, and L_{boostb}, respectively, to be stored

therein. The isolated boost power converter 700 comprises an input terminal 104 for receipt of an input voltage, V_{in}, which for example may be a DC voltage between 5 Volt and 100 Volt. The first and second boost inductors, L_{boosta}, and L_{boostb}, are both coupled to the input voltage at terminal 704. A first H-bridge transistor driver 706a is coupled to the first boost inductor, L_{boosta}, and a second H-bridge transistor driver 706b is coupled to the second boost inductors, L_{boostb}. Each of the first and second three legged EI cores 702a, 702b have associated primary and second transformer windings, PW_{1a} , PW_{2a} and SW_{1a}, SW_{2a} and PW_{1b} , PW_{2b} and SW_{1b}, SW_{2b}, respectively, in a topology similar to the topology discussed above in detail in connection with the first embodiment of the invention. However, only the center-tap 716 in-between the first and second series connected secondary transformer windings, SW_{1a} and $SW_{2a,}$ respectively, is coupled to a rectifying element in form of semiconductor diode D_f. The first and second series connected secondary transformer windings, $SW_{1b,}$ SW_{2b} of the second EI core 702b are not connected to a center-tap but each half-winding output is coupled in series with the corresponding secondary half-winding of the first EI core 702a. The isolated boost power converter 700 comprises a shared single rectification circuit 719 coupled to respective winding outputs of the first and second secondary windings SW_{1b} and SW_{2b}. The rectification circuit 719 is configured as a full-wave rectifier comprising four rectifying diodes D_1 - D_4 to produce a rectified converter output voltage V_{out} between positive and negative output voltage terminals or nodes 719, 721, respectively.

[0049] It is accordingly evident that the first and second primary transformer windings PW_{1-2a} and PW_{1-2b} are both coupled to separate drivers 706a and 706b, respectively, while the pair of first secondary transformer windings SW_{1a} and SW_{1b} are coupled in series between the center tap 716 and the rectification circuit 718 and the pair of second secondary transformer windings SW_{2a} and SW_{2b} likewise are coupled in series between the center tap 716 and the rectification circuit 718. This topology has the beneficial effect that voltage amplification, i.e. the ratio between the input voltage V_{in} and the rectified converter output voltage V_{out}, is doubled

compared to the topology disclosed on Figs. 1-5 due to the series connected pairs of first and second secondary windings. In addition, the shared "I" leg 740 provides further magnetics integration so as to reduce material costs, decrease size and increase efficiency due to flux cancellation in the shared "I" leg 740.

[0050] Furthermore, the first and second series connected secondary transformer windings, $SW_{1a,}$ SW_{2a} are configured to discharge magnetic energy stored in the first boost inductor, L_{boosta}, in a manner similar to one used in the above-mentioned first embodiment of the invention by a shared magnetic flux path comprising a first magnetic flux path extending through the first center leg 734a, and the first outer leg 732a and a second magnetic flux path extending through the first center leg 734a, and the second outer leg 736a. Likewise, the first and second series connected secondary transformer windings, $SW_{1b,}$ SW_{2b} of the upper EI core 702b are configured to discharge magnetic energy stored in the second boost inductor, L_{boostb}, through a shared magnetic flux path in the upper EI core 702b.

[0051] Fig. 8 is a graph 800 depicting measurement data from an experimental isolated boost power converter in accordance with the above-described first embodiment of the invention. The experimental isolated boost power converter had the following key data:

Windings on $L_{boost} = 2$

primary transformer windings, $PW_{1-2} = 2$

secondary transformer windings, $SW_1 + SW_2 = 8$

DC input voltage, V_{in} = 25 Volt

Load resistance, R_L= 68.2 ohm

Core type: ELP64 available from manufacturer EPCOS AG.

Core material: N87

Air gap height (at center leg) = 0.5 mm.

[0052] The graph data were acquired by maintaining V_{in} at 25 Volt and sweeping a duty cycle, D, of a Pulse Width Modulated (PWM) driver control signal from 0 to 0.75 and then back to 0 over a time period of 4 seconds. The time variable is indicated along the x-axis 805. The corresponding duty cycle, D, is indicated on the right-hand vertical scale 803 and the measured

rectified converter output voltage, V_{out}, indicated on the left-hand vertical scale in Volts. The substantially linear correlation between the duty cycle and the rectified converter output voltage, V_{out}, is evident, and is for D>0.5 in accordance with equation (1) above. It is also noticeable that the rectified converter output voltage, $V_{out,}$ is continuous across the boundaries at D = 0.5 between start-up mode operation and normal boost mode operation. For D = 0.75, the following electrical data were measured, input current (at V_{in}) = 27.94 A, V_{out} = 205.11 Volt, output current = 3.006 A.

[0053] Hence, the present measurement data confirms the capability of the present experimental isolated boost power converter to start-up (D<0.5) and proceed to normal boost operation (D>0.5) in a well-behaved manner without any need for a separate flyback winding or other dedicated start-up circuitry.

CLAIMS

1. An isolated boost power converter comprising:

- a magnetically permeable multi-legged core,

- an input terminal for receipt of an input voltage, Vin,

- a boost inductor being wound around a first leg of the magnetically permeable multi-legged core,

- the boost inductor being electrically coupled between the input terminal and a driver to be alternatingly charged and discharged with magnetic energy,

- the driver having a driver output coupled to a primary transformer winding wound around a second leg of the magnetically permeable transformer core,

- the driver being configured to generate a primary voltage to the primary transformer winding in accordance with a driver control signal,

- first and second series connected secondary transformer windings with a center-tap arranged in-between and wound around separate legs of the magnetically permeable multi-legged core,

- a rectification circuit electrically coupled to respective outputs of the first and second secondary transformer windings to provide a rectified converter output voltage, Vout; wherein

- in a first discharge state, the magnetic energy stored in the boost inductor is discharged by directing a discharge current from the boost inductor through the primary transformer winding,

- in a second discharge state, the magnetic energy stored in the boost inductor is discharged by discharging a magnetic flux through the first and second secondary transformer windings.

2. An isolated boost power converter according to claim 1, wherein the first and second secondary transformer windings are coupled in parallel from the center-tap between first and

second series connected secondary transformer windings to the rectified converter output voltage, V_{out}.

3. An isolated boost power converter according to claim 1 or 2, wherein the second discharge state is automatically entered when the driver enters a non-conducting or off-state such as when a duty cycle of a pulse width modulated driver control signal is less than 0.5.

4. An isolated boost power converter according to any of the preceding claims, wherein the boost converter is configured to:

- during the first discharge state, magnetically decoupling the boost inductor from the first and second secondary transformer windings to deliver the magnetic energy to the primary transformer winding;
- during the second discharge state, magnetically coupling the boost inductor to the first and second secondary transformer windings through a shared flux path in the magnetically permeable multi-legged core.

5. An isolated boost power converter according to any of the preceding claims, wherein the first and second secondary transformer windings are configured to discharge the magnetic energy stored in the boost inductor by supplying a discharge current to the rectified converter output voltage, V_{out}, so as to transfer energy to the output - Whereby the first and second secondary transformer windings act as flyback windings.

6. An isolated boost power converter according to any of the preceding claims, wherein the magnetically permeable multi-legged core comprises:

- a center leg, having an air gap arranged therein,
- a first outer leg and a second outer leg;
- wherein the boost inductor is magnetically coupled to the center leg to store the magnetic energy therein and the first and second secondary transformer windings being wound around the first and second outer legs, respectively.

7. An isolated boost power converter according to claim 6, wherein the boost inductor is wound around the center leg.

8. An isolated boost power converter according to claim 6 or 7, wherein the air gap of the center leg has a height between 0.1 mm and 1.0 mm.

9. An isolated boost power converter according to any of claims 6-8, wherein the primary transformer winding comprises first and second series connected half-windings wound around the first and second outer legs, respectively, of the magnetically permeable multi-legged core.

10. An isolated boost power converter according to any of the preceding claims, wherein the driver comprises a full-bridge transistor driver having a first and second complementary driver outputs coupled to respective ends of the primary transformer winding.

11. An isolated boost power converter according to any of claims 1-9, comprising a first boost inductor and a second boost inductor;

- the first boost inductor being coupled between the input terminal and a first transistor driver output coupled to a first end of the primary transformer winding,
- the second boost inductor being coupled between the input terminal and a second transistor driver output coupled to a second end of the primary transformer winding.

12. An isolated boost power converter according to any of claims 1-9, wherein the boost inductor comprises a first half-winding and a second half-winding of the primary transformer winding to provide an integrally formed boost inductor and primary winding.

13. An isolated boost power converter according to any of the preceding claims, further comprising a rectifying element electrically coupled to the center-tap to conduct a discharge

current, during the second discharge state, from the first and second secondary transformer windings to the rectified converter output voltage, V_{out}.

14. An isolated boost power converter according to any of claims 1-12, wherein the rectification circuit comprises a center-tapped rectifier wherein:

- the center-tap is electrically connected to a negative rectified converter output voltage or the rectified converter output voltage, V_{out},
- the respective outputs of the first and second secondary transformer windings are coupled to the opposite output voltage to the one electrically coupled to the center-tap through first and second rectifying elements.

15. An isolated boost power converter according to any of the preceding claims, wherein the rectification circuit comprises a voltage doubler circuit.

16. An isolated boost power converter according to claim 13, wherein the rectifying element and/or the rectification circuit comprises one or more semiconductor diode(s), diode-coupled transistor(s), synchronously controlled transistor switch(es).

17. An isolated boost power converter according to claim 9, further comprising:

- a second magnetically permeable multi-legged core,
- a second boost inductor magnetically coupled to a center leg of the second magnetically permeable multi-legged core to store magnetic energy therein,
- the second boost inductor being electrically coupled between the input terminal and a second driver to be alternatingly charged and discharged with magnetic energy,
- the second driver having a second driver output coupled to a second primary transformer winding wound around a first outer leg and a second outer leg of the second magnetically permeable transformer core,
- the second driver being configured to generate a second primary voltage to the second primary transformer winding in accordance with the driver control signal,

- first and second secondary transformer windings wound around the first outer leg and the second outer leg, respectively, of the second magnetically permeable multi-legged core, wherein:

- the first secondary transformer winding of the second magnetically permeable multi-legged core is coupled in series between the rectification circuit and the output of the first secondary transformer winding of the magnetically permeable multi-legged core; and

- the second secondary transformer winding of the second magnetically permeable multi-legged core is coupled in series between the rectification circuit and the output of the second secondary transformer winding of the magnetically permeable multi-legged core such that:.

- in the first discharge state, the respective magnetic energies stored in the first and second boost inductors are discharged by directing respective discharge currents from the respective boost inductors through the respective primary transformer windings,

- in the second discharge state, the respective magnetic energies stored in the respective boost inductors are discharged by discharging respective magnetic fluxes through the respective first and second secondary transformer windings.

18. An isolated boost power converter according to claim 17, wherein the first and second magnetically permeable multi-legged cores share a common magnetic flux path extending through a shared magnetically permeable leg.

19. An isolated boost power converter according to claim 18, wherein the first and second magnetically permeable multi-legged cores are configured to provide magnetic flux cancellation or suppression in the common magnetically permeable leg.

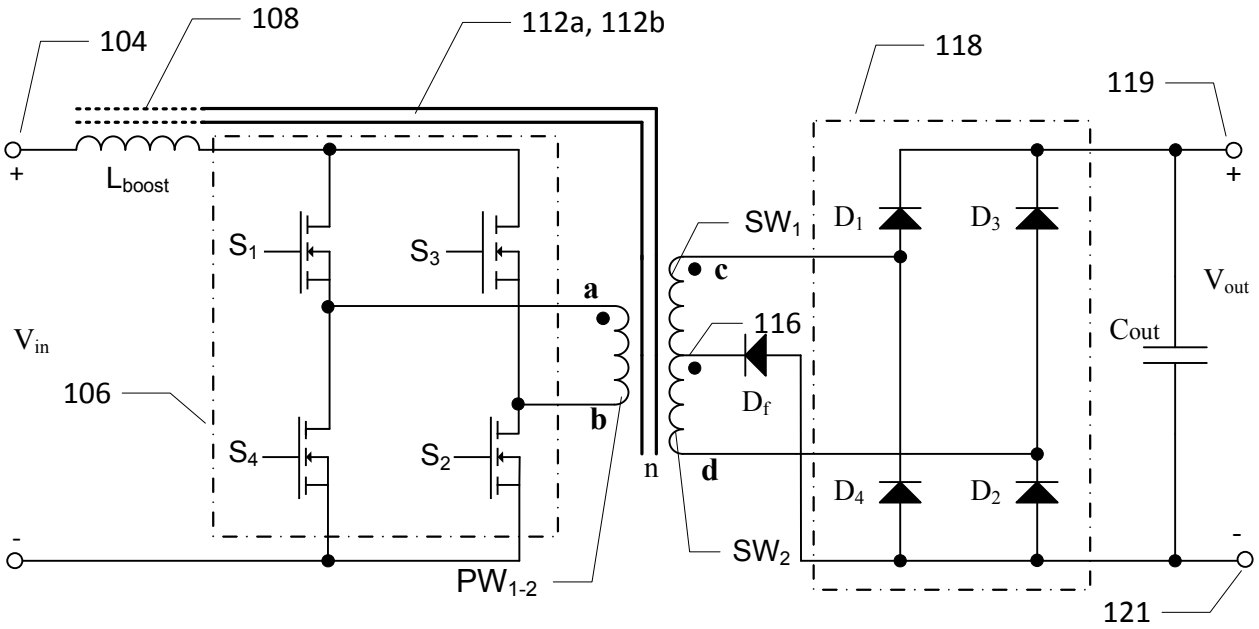
20. An isolated boost power converter according to any of the preceding claims, wherein the driver control signal comprises a pulse width modulated signal having an adjustable duty cycle, D.

21. A method of generating a rectified converter output voltage, V_{out} from an input voltage, V_{in}, by an isolated boost power converter according to any of the preceding claims, comprising steps of:

- generating a pulse width modulated driver control signal,
- supplying the pulse width modulated driver control signal to the driver,
- gradually increasing a duty cycle, D, of the pulse width modulated driver control signal from below 0.5, preferably below 0.1, to a value above 0.5, preferably between 0.55 and 0.99,
- adjusting the duty cycle, D, to a desired value to reach a desired or target AC or DC voltage at the rectified converter output voltage, V_{out}.

ABSTRACT

The present invention relates to an isolated boost power converter comprising a boost inductor being wound around a first leg of a magnetically permeable multi-legged core. The boost inductor is electrically coupled between an input terminal of the boost converter and a transistor driver to be alternatingly charged and discharged with magnetic energy. A first and second series connected secondary transformer windings with a center-tap arranged in-between are wound around separate legs of the magnetically permeable multi-legged core. In a first discharge state, the magnetic energy of the boost inductor is discharged by directing a discharge current from the boost inductor through a primary transformer winding and in a second discharge state, the magnetic energy of the boost inductor is discharged by discharging a magnetic flux through the first and second secondary transformer windings. In this manner, the secondary transformer windings can replace the traditional separate flyback winding used for start-up purposes of isolated boost power converters.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108
112a, 112b
118
119
+
L_{boost}
S_1
S_3
SW_1
D_1
D_3
+
a
c
V_{out}
V_{in}
116
C_{out}
106
D_f
b
S_4
S_2
n
d
D_4
D_2
-
SW_2
-
PW_{1-2}
121

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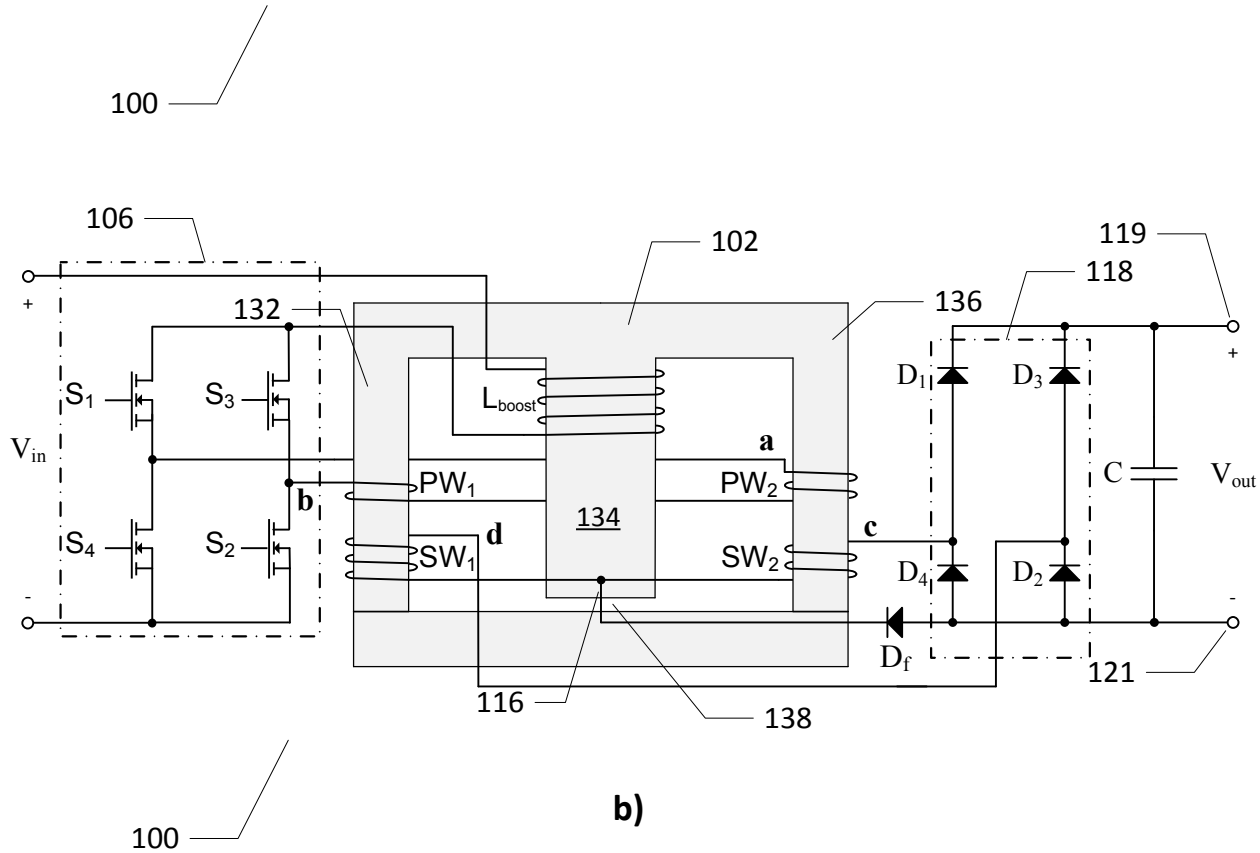
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PW_2
C
V_{out}
b
134
S_4
S_2
d
SW_1
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SW_2
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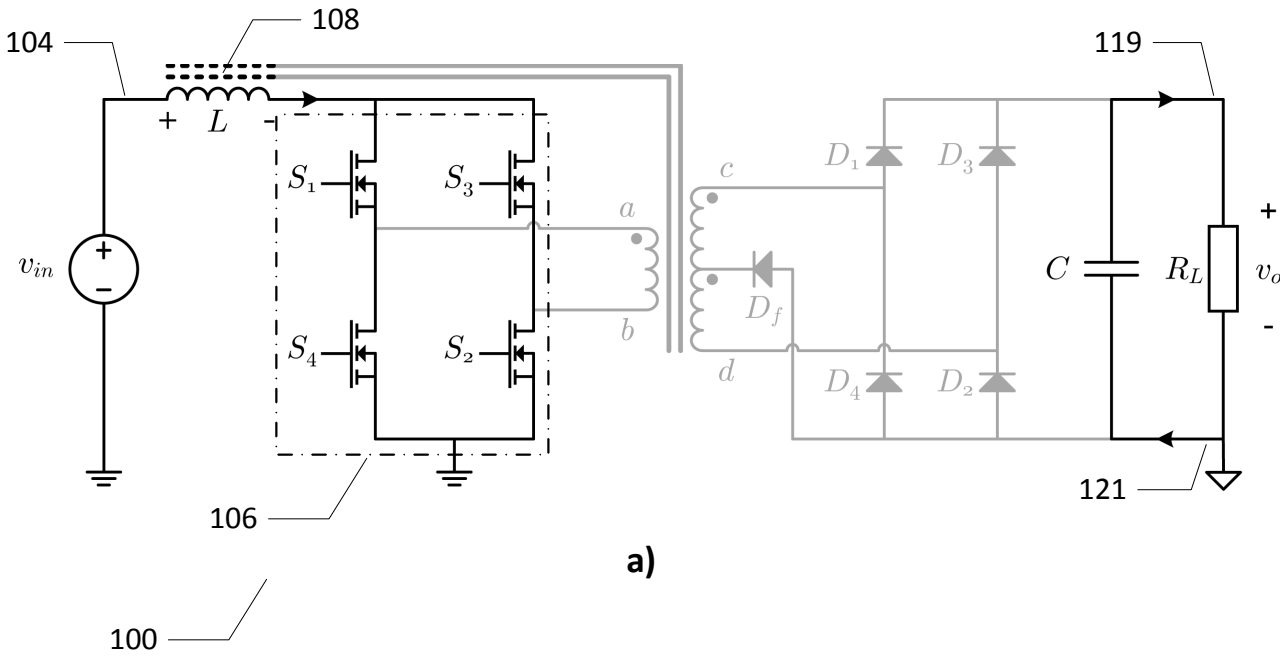
D_2
-
D_f
-
116
121
138
100

b)

Fig. 1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L
S_1
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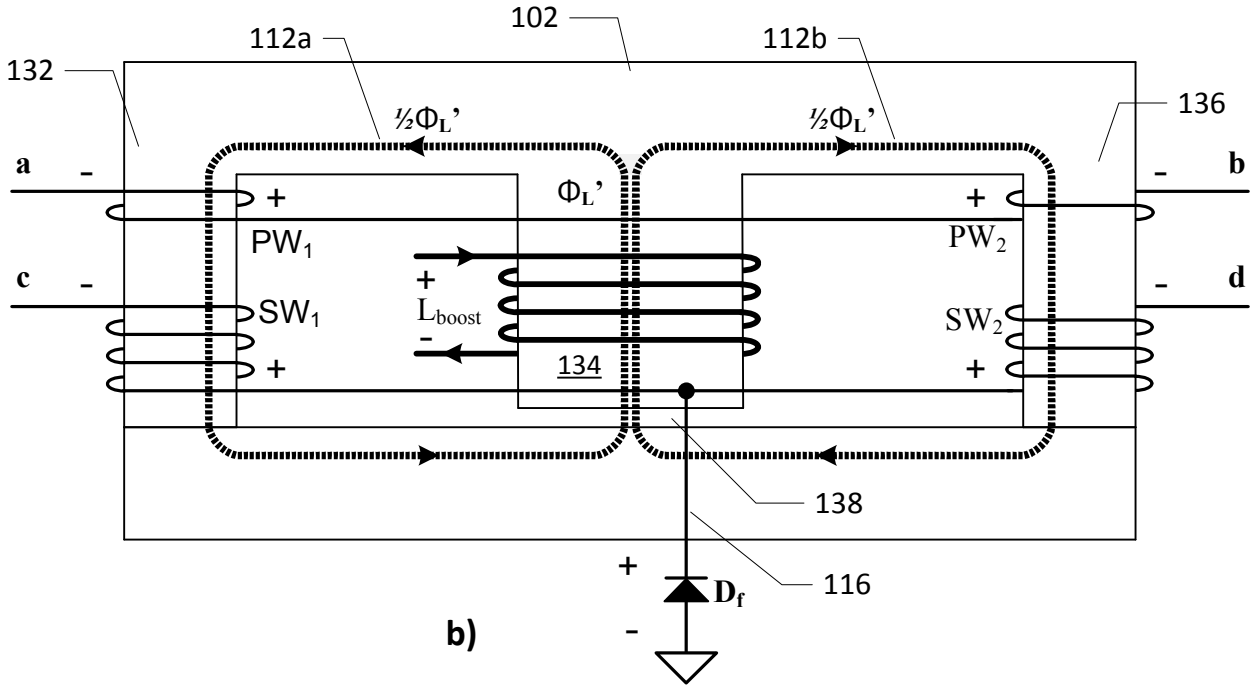
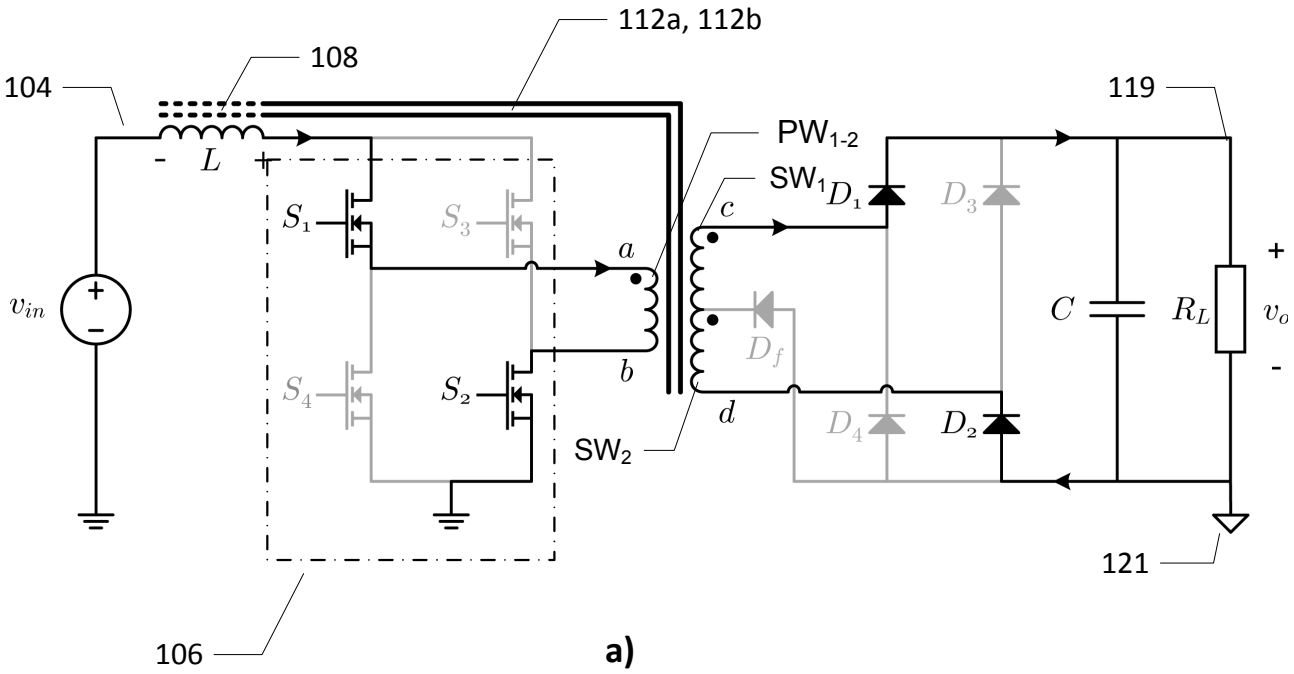
121
100

a)


102
112a
112b
132
136
½Φ_L'
½Φ_L'
a
b
c
d
Φ_L'
PW1
PW2
SW1
SW2
L_boost
134
138
116
D_f

b)

Fig. 2


112a, 112b
108
104
119
PW1-2
SW1
L
S1
S3
a
c
D1
D3
vin
C
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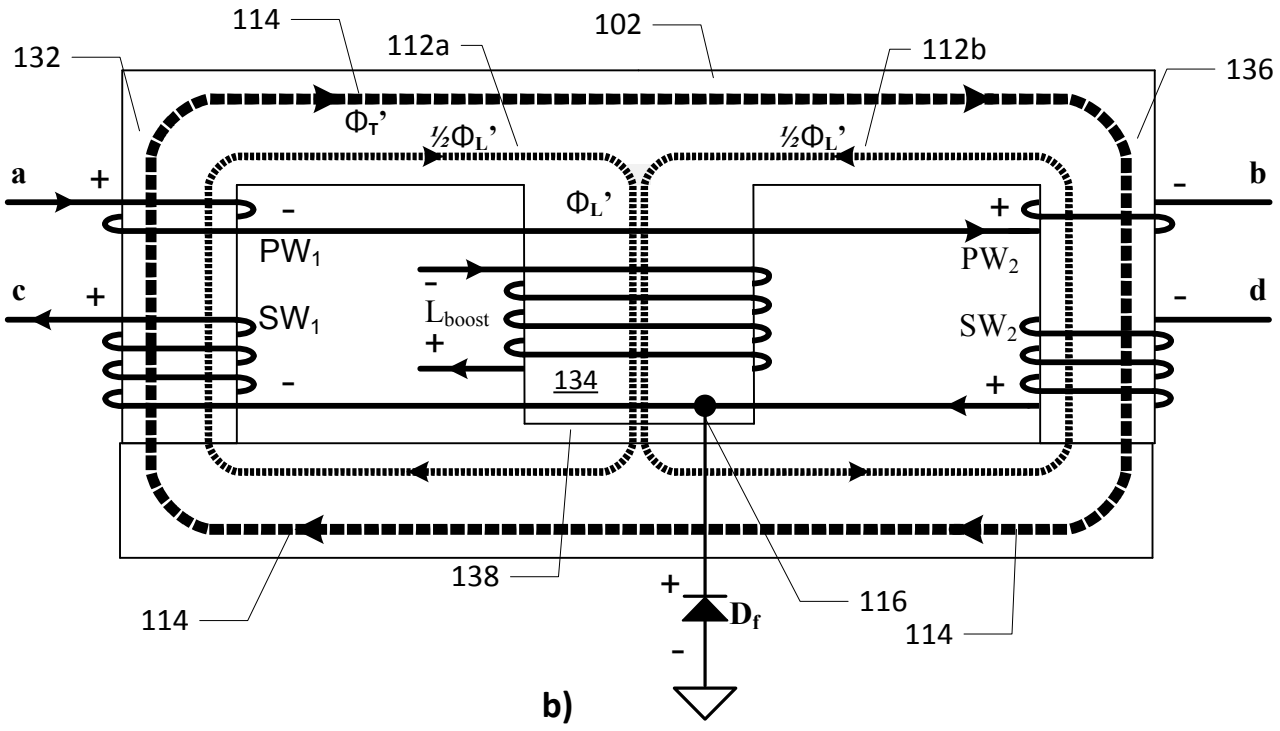
Df
b
S4
S2
d
D4
D2
SW2
121
106

a)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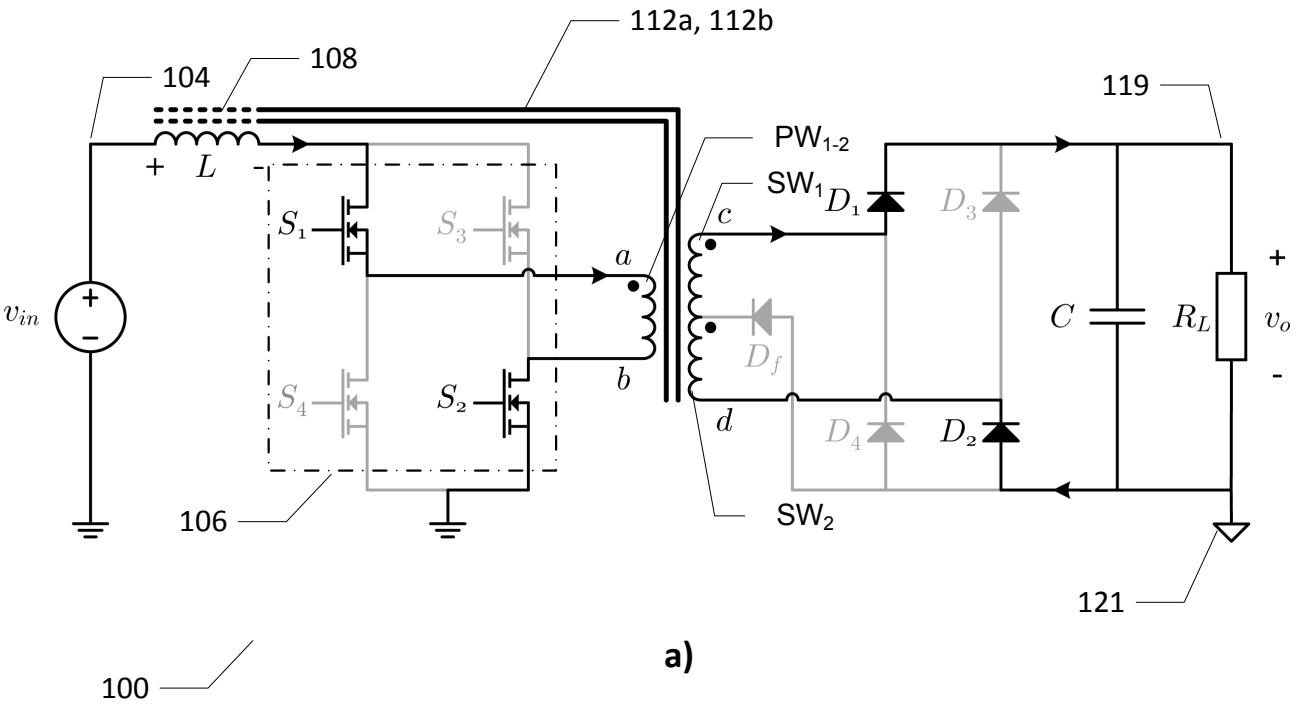
102
132
112a
112b
136
Φт'
½ΦL'
½ΦL'
a
b
ΦL'
PW1
PW2
c
d
SW1
Lboost
SW2
134
138
116
114
114
Df

b)

Fig. 3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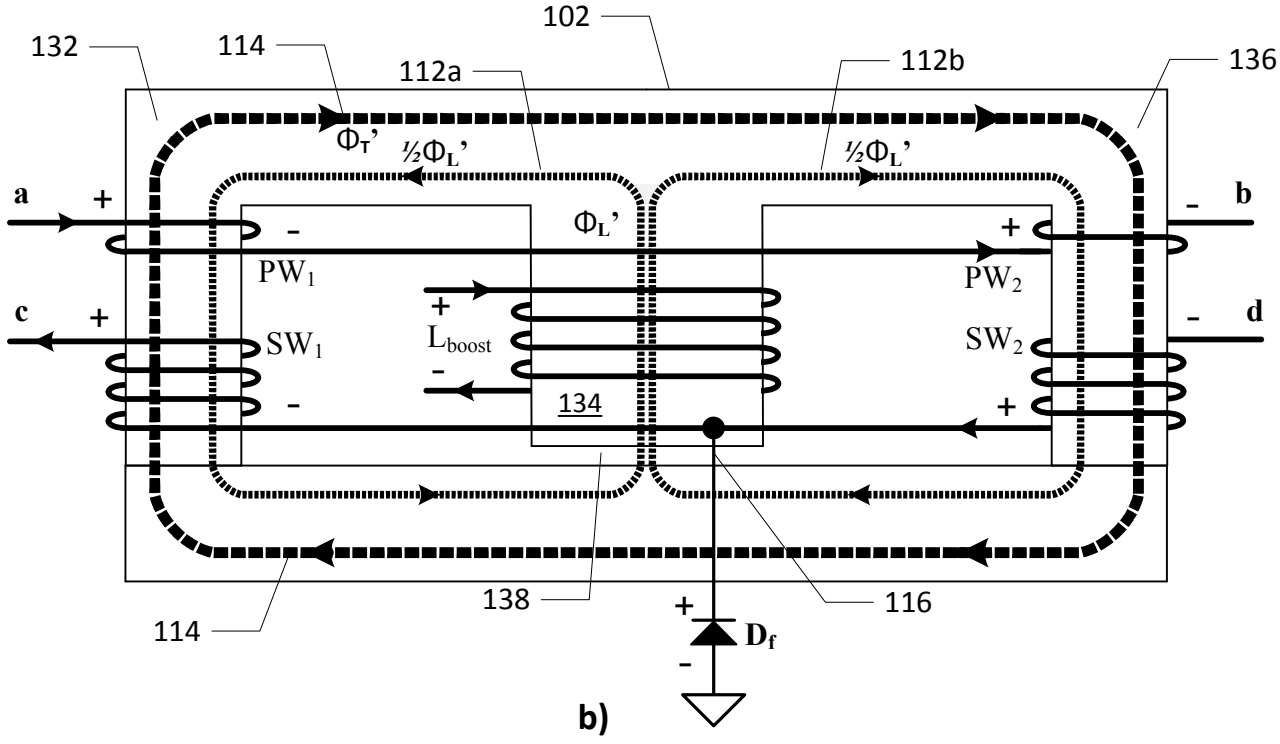
108
119
PW1-2
SW1
L
S1
S3
a
c
vin
D1
D3
C
RL
vo
Df
S4
S2
b
d
D4
D2
106
SW2
121
100

a)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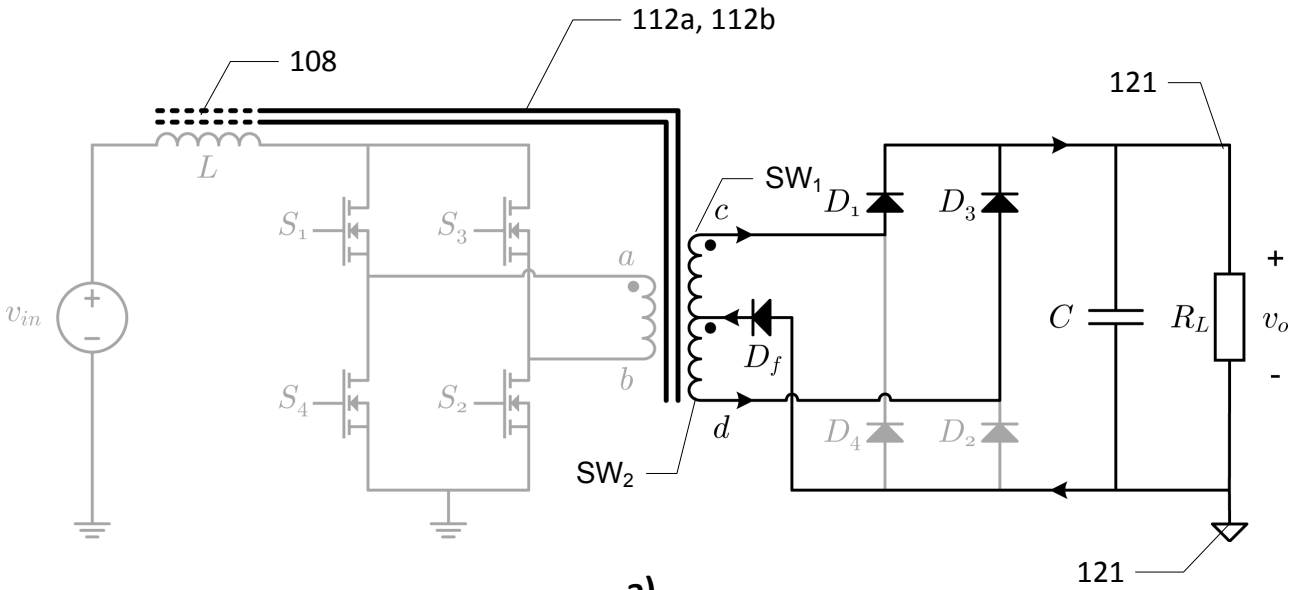
132
114
112a
112b
136
Φτ'
½ΦL'
½ΦL'
a
b
ΦL'
PW1
PW2
c
d
SW1
Lboost
SW2
134
138
116
114
Df

b)

Fig. 4


112a, 112b
108
121
L
SW1
D1
D3
c
S1
S3
a
vin
+
−
C
RL
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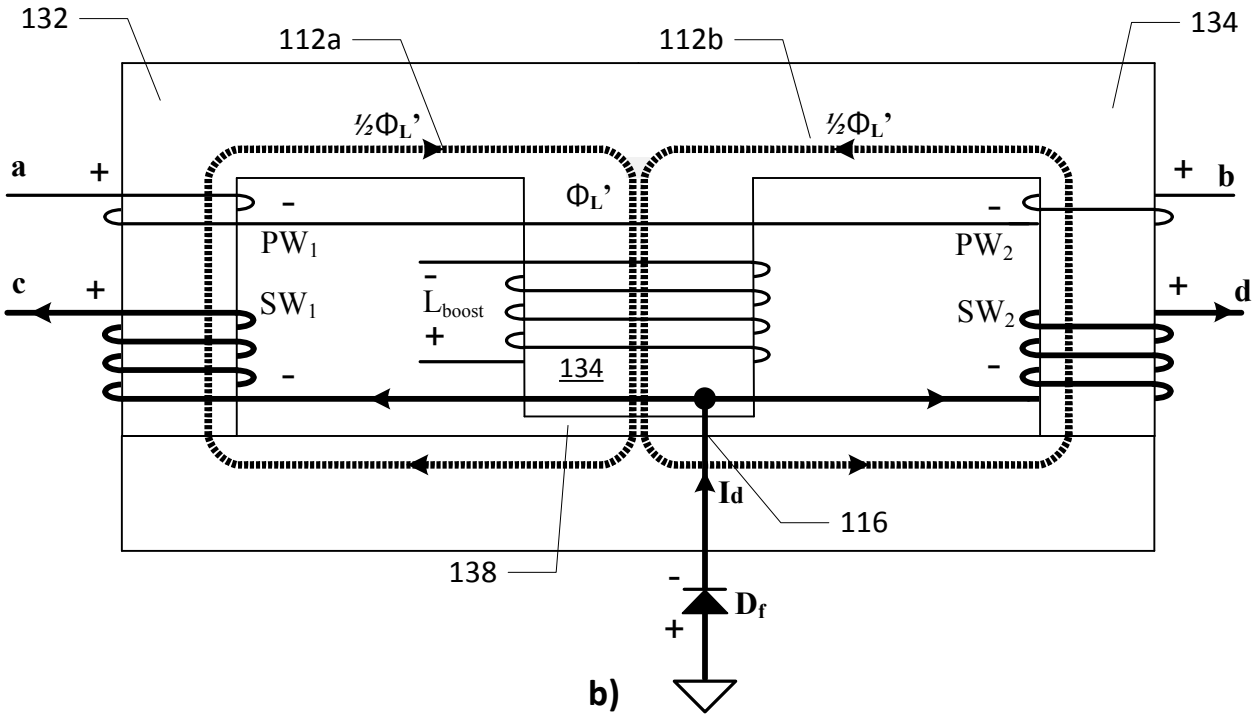
+
-
Df
b
S4
S2
d
D4
D2
SW2
121

a)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112a
112b
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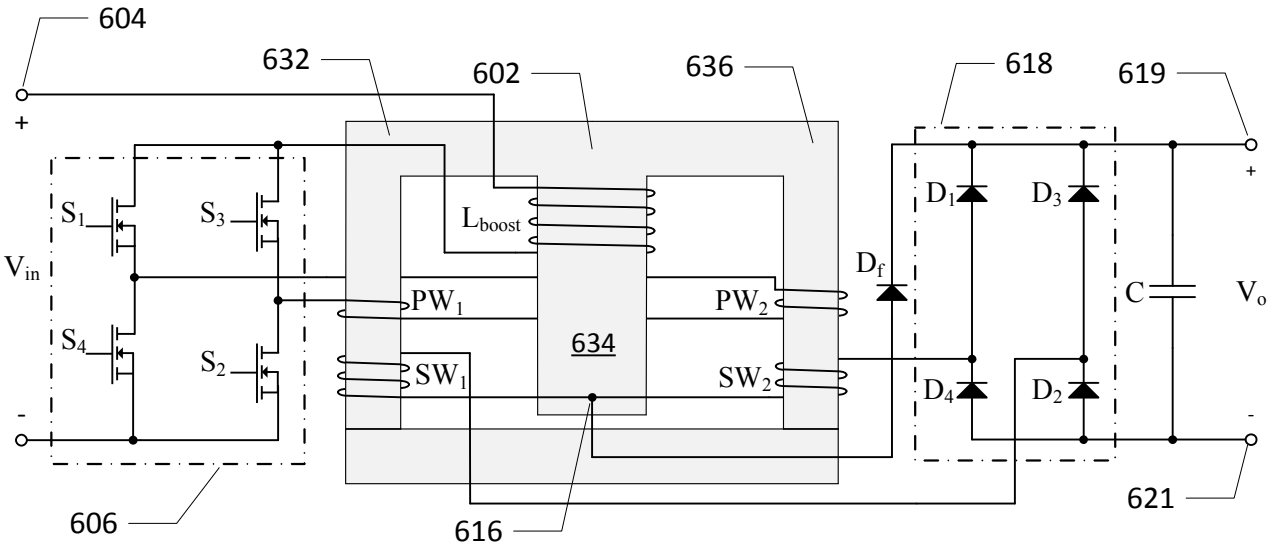
½ΦL'
½ΦL'
a
+
+
b
-
ΦL'
-
PW1
PW2
c
+
SW1
Lboost
+
SW2
+
d
-
134
-
Id
116
138
-
Df
+

b)

Fig. 5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632
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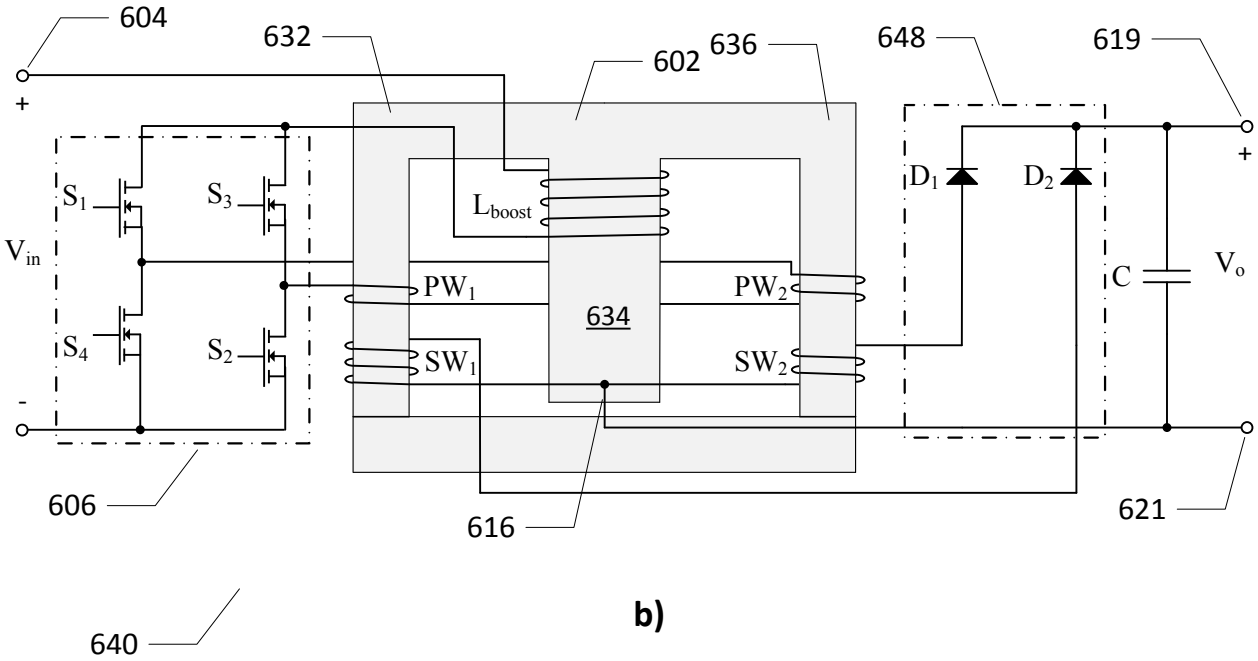
619
+
V_{in}
S_1
S_3
S_4
S_2
-
L_{boost}
PW_1
PW_2
SW_1
SW_2
634
D_f
D_1
D_3
D_4
D_2
C
V_o
606
616
621

a)


604
632
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636
648
619
+
V_{in}
S_1
S_3
S_4
S_2
-
L_{boost}
PW_1
PW_2
SW_1
SW_2
634
D_1
D_2
C
V_o
606
616
621
640

b)

Fig. 6

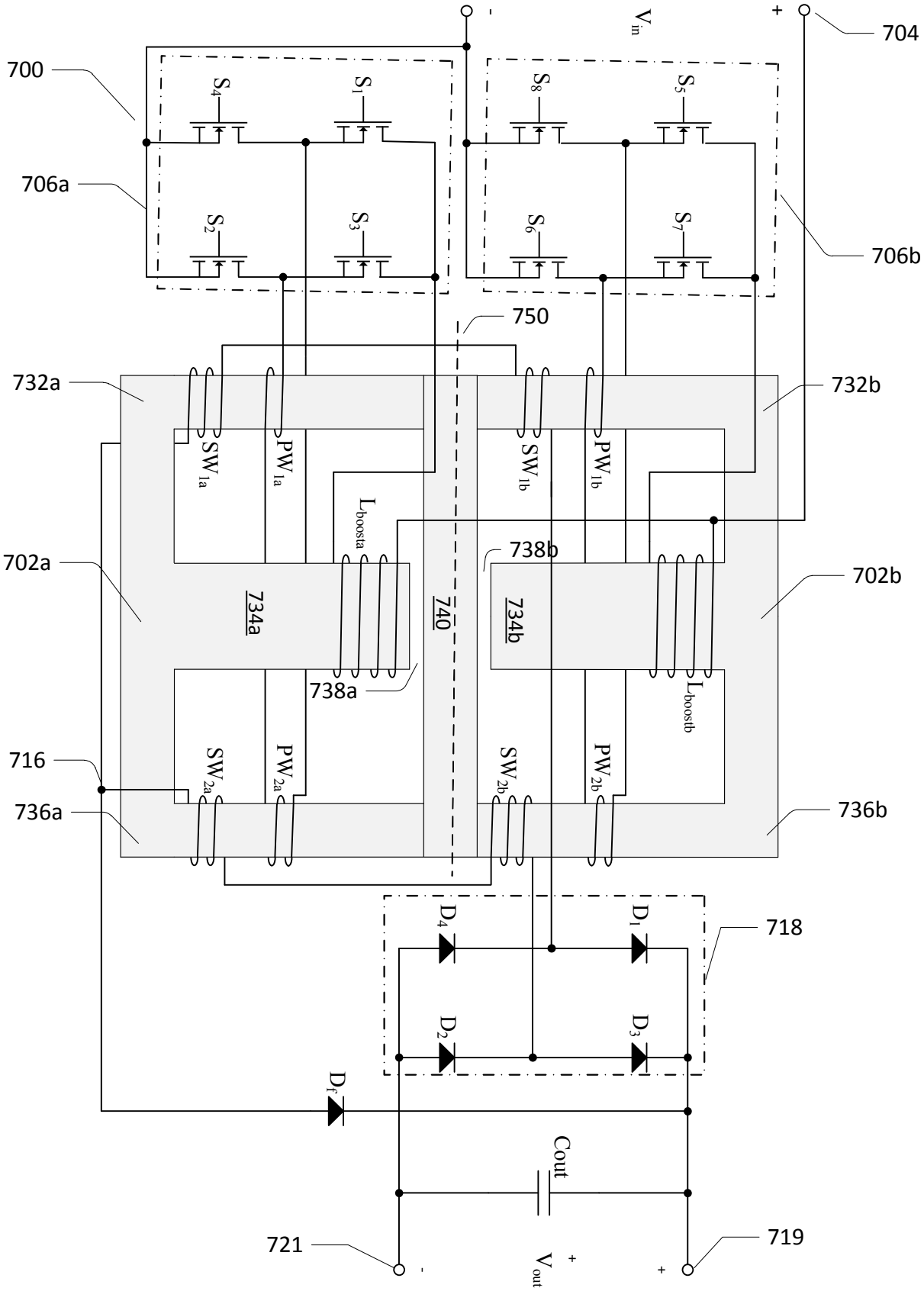
700
704
706a
706b
750
732a
732b
702a
702b
738b
738a
716
736a
736b
718
721
719
V_{in}
V_{out}
S_1
S_2
S_3
S_4
S_5
S_6
S_7
S_8
SW_{1a}
PW_{1a}
SW_{1b}
PW_{1b}
L_{boosta}
L_{boostb}
SW_{2a}
PW_{2a}
SW_{2b}
PW_{2b}
734a
734b
740
D_1
D_2
D_3
D_4
D_f
Cout

Fig. 7

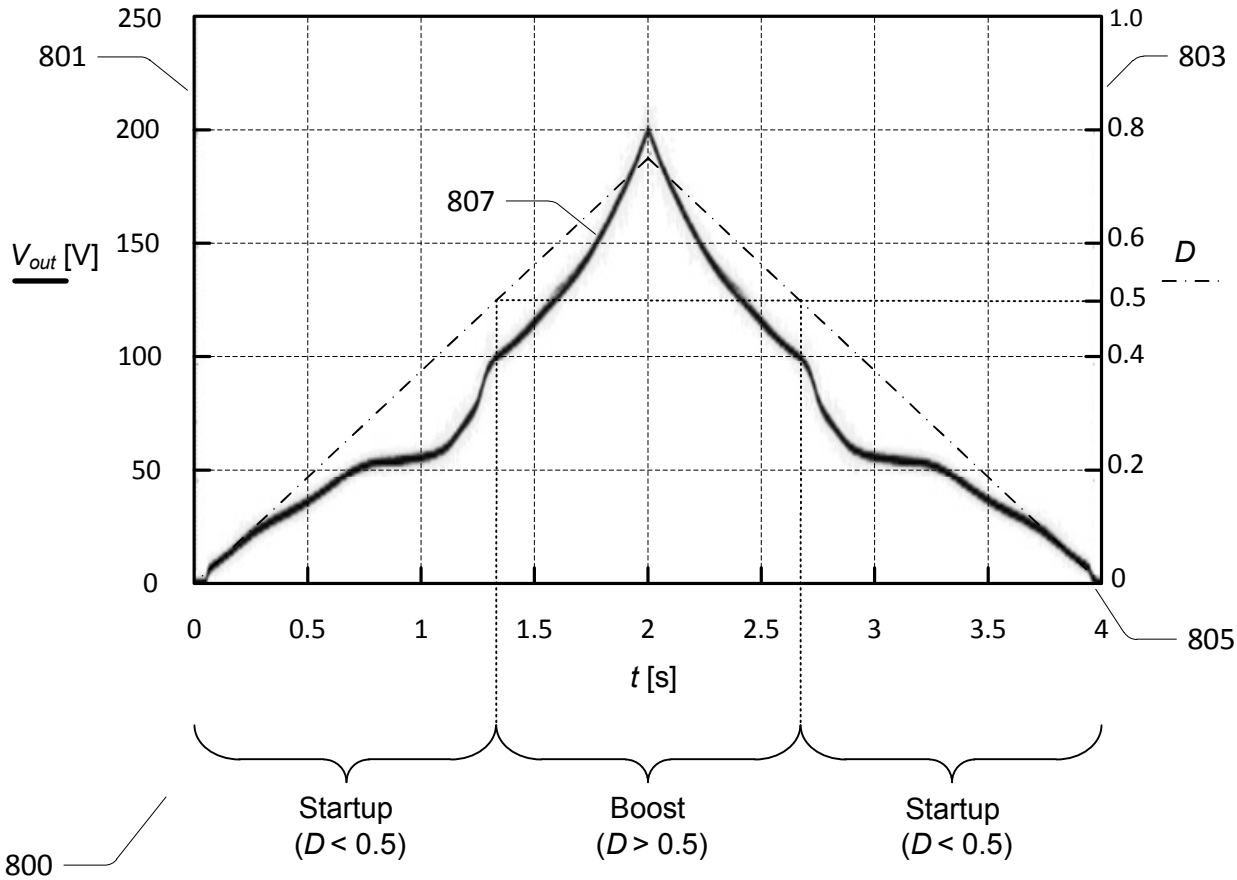
250
200
150
100
50
0
801
V_{out} [V]
807
1.0
0.8
0.6
0.5
0.4
0.2
0
803
D
805
0
0.5
1
1.5
2
2.5
3
3.5
4
t [s]
800
Startup
(D < 0.5)
Boost
(D > 0.5)
Startup
(D < 0.5)

Fig. 8

Appendix A11

[A11] J. C. Hernández B., **G. Sen**, M. C. Mira A., O. C. Thomsen, M. A. E. Andersen, "Primary parallel isolated boost converter with extended operating voltage range," ECRES 2012 (**Accepted)**.

Primary Paralleled Isolated Boost Converter with Extended Operating Voltage Range

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Abstract

Applications requiring wide input and output voltage range cannot often be satisfied by using buck or boost derived topologies. Primary paralleled isolated boost converter (PPIBC) [1]-[2] is a high efficiency boost derived topology. This paper proposes a new operation mode for extending the input and output voltage range in PPIBC. The proposed solution does not modify PPIBC power stage, the converter gain is modified instead by short circuiting one of the paralleled connected primary windings present in this topology.

Keywords: Isolated boost, battery, extended range.

Nomenclature:

R_g	Source series resistance
V_g	Source voltage
$R_{D_{Bat}}$	Battery dynamic resistance
$V_{OC_{Bat}}$	Battery open circuit voltage
r_L	Inductor parasitic resistance
r_{MP}	Primary MOSFET's on resistance
r_p	Transformer primary resistance
r_S	Transformer secondary resistance
r_{MS}	Secondary MOSFET's on resistance

1. Introduction

In this paper an alternative solution with an extended voltage operation range is proposed based on modifying the operating mode of PPIBC, which has been reported [1]-[2] as a high efficient solution in low voltage high current applications. This topology, derived from the simple isolated boost converter, increases the efficiency by splitting the primary current through two parallel primary stages (Figure 1). This approach results in reduced ac current loops which helps reducing the power stage layout stray inductances. Together with the transformer leakage inductances, stray inductances increase the switching loses. In addition, the two transformer secondary windings are connected in series which reduces the number of turns on the secondary side for individual transformers allowing for an easier magnetic component design. The primary switches in each parallel stage are driven with identical gate signals. Moreover, the two stages share the input inductor as well as the input and output filters, which makes this topology a simpler solution. Due to the transformer series connection on the secondary side the two currents flowing through the two primary stages are forced to be equal during the inductor discharge state. In order to balance the current between the primary stages a current balancing transformer (CBT) [3] is inserted. This component is implemented as two inversely coupled inductors that present high impedance in case of current imbalance, keeping the current in each parallel stage equal. The converter schematic and steady state operating waveforms are presented in (Figure 1). The voltage gain is given in (1).

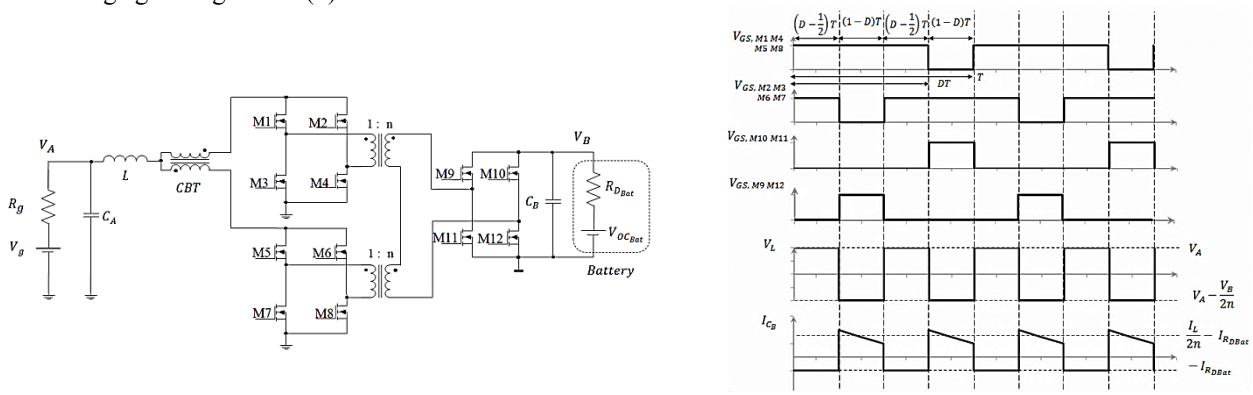


Figure 1. PPIBC schematic and steady state waveforms

$$M(D) = \frac{V_B}{V_A} = n \cdot \frac{1}{(1-D)} \tag{1}$$

Boost derived topologies can ideally increase their output voltages up to very high values when the primary switches' duty cycle approaches 100%. Therefore it is possible to adjust the turn ratio of the transformer such that the full operating range can be covered by adjusting the duty cycle. However, operating the converter with extreme duty cycles will significantly increase the rms current stress in the components, which will affect the converter efficiency. Therefore, a change in converter operation mode could be utilized to keep the switch duty cycles in acceptable values.

2. Extended operating voltage range

The state-of-the art solution for extended voltage range in isolated boost converters has been presented in the literature [4]-[5]. The solution in [4] proposes an auxiliary winding in the input inductor that will provide flyback operation to the converter, extending the operating voltage range and solving the intrinsic start up problems in boost derived topologies. However, this is not an efficient solution in high power applications and makes the manufacturing process of the input inductor more complicated because extensive interleaving techniques will have to be adopted to increase the coupling coefficient of the flyback winding.

This paper presents an efficient solution for extending the voltage range of PPIBC by implementing a new operation mode where the two upper side MOSFETs in one of the parallel stages are shut down while the lower side switches are kept in conduction mode. This new operation mode effectively reduces the equivalent converter conversion ratio by short circuiting the primary winding in one of the primary stages which deactivates the corresponding transformer.

As in the auxiliary flyback winding configuration, the main drawback of this solution is the increased voltage stress on the primary switches during extended operation (2). This fact will increase the requirement for the primary switch breakdown voltage, consequently increasing the device on resistance which affects the converter efficiency.

$$V_{DS_{PPIBC}} = \frac{V_B}{2 \cdot n} \qquad V_{DS_{Flyback}} = V_A + \frac{V_B}{2 \cdot n} \qquad V_{DS_{PPIBC\_Extended}} = \frac{V_B}{n} \tag{2}$$

However this is an attractive solution in applications with variable output voltage where the extended mode will be operated only under minimum output voltage. For example in battery applications when a heavy load condition is applied to the battery, the battery voltage will collapse (acceleration event in an electric vehicle). (Figure 2) and (Figure 3) present the converter steady state waveforms and voltage gain during extended voltage range operation. (3) gives the modified voltage conversion ratio.

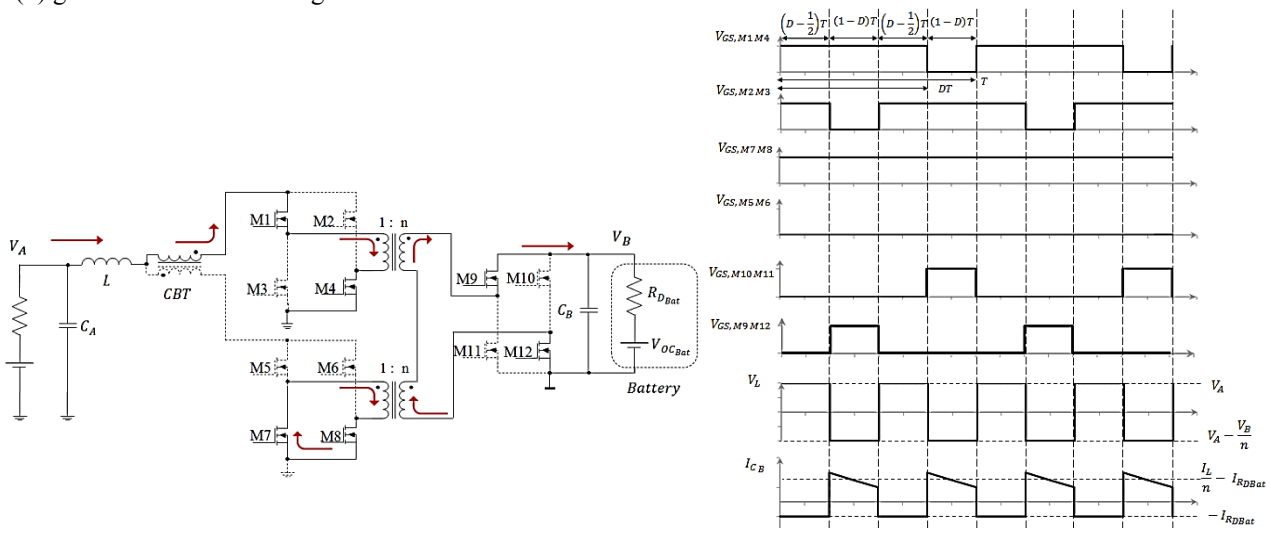
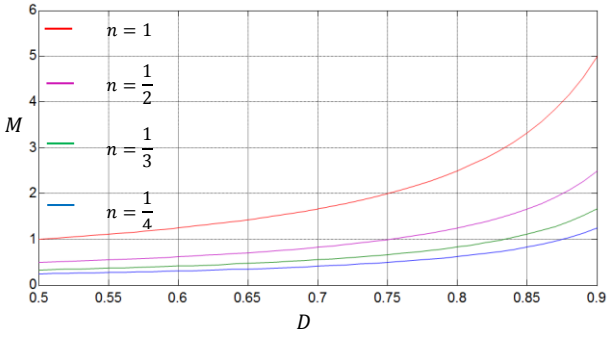


Figure 2. PPIBC steady state waveforms during extended voltage operation



$$M(D) = \frac{V_B}{V_A} = n \cdot \frac{1}{2 \cdot (1 - D)} \tag{3}$$

Figure 3. Converter voltage gain during extended operation mode for different transformer turns ratios.

3. Simulation of PPIBC with extended voltage range operation

The proposed solution is analyzed by performing several LTspice simulations with the operating conditions shown in Table 1. (Figure 4) presents a simulation result where the inductor current level is fixed at $20A$ during closed loop operation of the converter. It can be observed that during the transition the current deviates from the reference value until the loop is able to compensate the error. The deviation in the current during the transition is caused by the change in the converter steady state conditions and the sensitivity of the inductor current to duty cycle perturbations as shown in [6]. This will increase the components' current stress which reduces the converter reliability.

Table 1 Parameters of the converter

Source voltage	30 V
Battery terminal voltage	24 V
Transformer turn ratio	3:1
Inductor	13.5 µH
Capacitor A	40 µF
Capacitor B	120 µF
Switching frequency	50 kHz
Source output resistance	10 mΩ
Battery dynamic resistance	60 mΩ

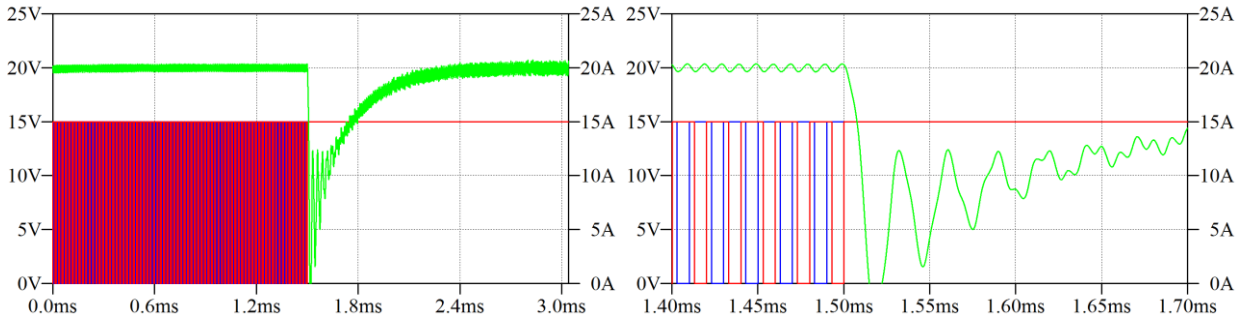


Figure 4. Simulated transition from normal operation mode to extended operation mode (left) and detailed zoomed of the transition (right). Converter input current I_g (green), M1 and M3 gate signal (red and blue).

4. Transition with pre-calculated steady-state duty cycle

The current stress during transition time can be reduced if a steady state duty cycle pre-calculation is performed based on an accurately derived model of the converter. In battery loading applications, as presented in [6]-[7], the duty cycle-to-inductor current transfer function is heavily affected by the converter parasitic resistances due to the low value of the battery dynamic resistance. (Figure 6) present the inductor charging and discharging states during extended voltage range operation.

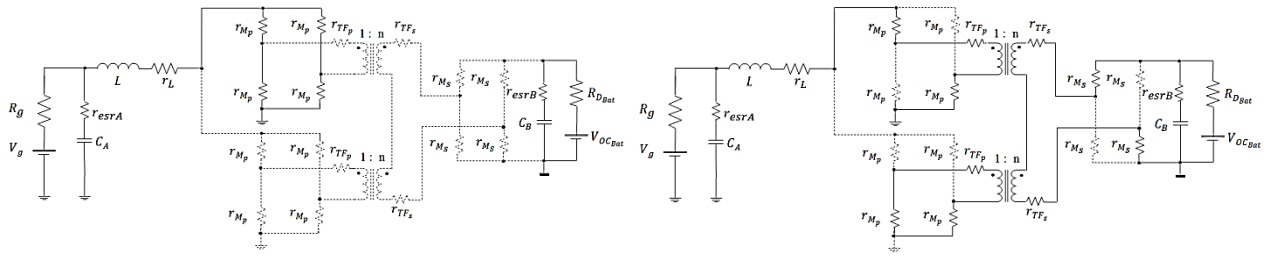


Figure 6. PPIBC conduction states during extended voltage range operation. (a) inductor charging subinterval, (b) inductor discharging subinterval

Based on the conduction states in (Figure 6) a new model can be obtained for the extended operating voltage mode. In this way, the converter duty cycle can be calculated prior to the transition between operating modes by using (4).

$$D = 2 \cdot \left(1 - \frac{I_L \cdot \left(R_g + \frac{R_{D_{Bat}}}{{N_e}^2} + r_{eq2} \right) + \frac{V_{OC_{Bat}}}{N_e} - V_g}{I_L \cdot \left(\frac{R_{D_{Bat}}}{{N_e}^2} + r_{eq2} - r_{eq1} \right) + \frac{V_{OC_{Bat}}}{N_e}} \right) \tag{4}$$

Where N_e corresponds to the effective transformer ratio and equivalent resistances r_{eq1} and r_{eq2} are defined as shown in (5) for normal operating mode and (6) for extended operating mode.

$$N_e = 2 \cdot n \qquad r_{eq1} = r_L + r_{M_P}/2 \qquad r_{eq2} = r_L + r_{M_P} + \frac{r_P}{2} + \frac{2r_S}{(2n)^2} + \frac{2r_{M_S}}{(2n)^2} \tag{5}$$

$$N_e = n \qquad r_{eq1} = r_L + r_{M_P} \qquad r_{eq2} = r_L + 4r_{M_P} + 2r_P + \frac{2r_S}{n^2} + \frac{2r_{M_S}}{n^2} \tag{6}$$

(Figure 7) shows a mode transition event where the controller has been set to produce the pre-calculated duty cycle before the transition event between operating modes.

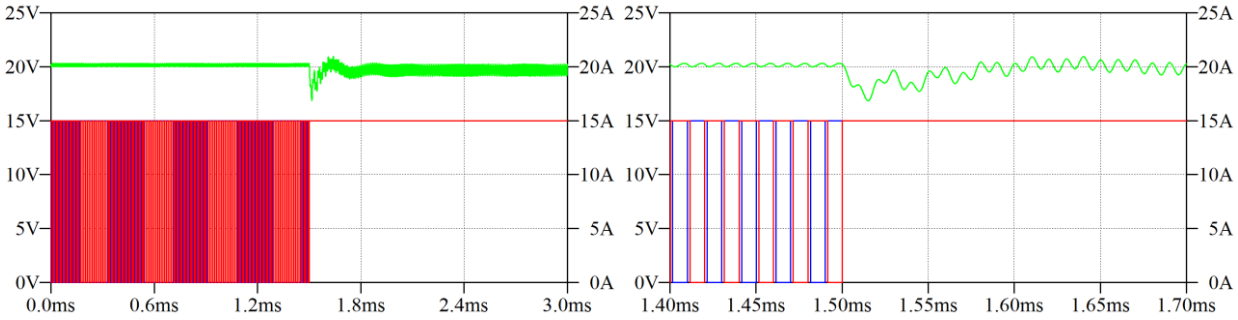


Figure 7. Simulated transition between operating modes with pre-calculated steady state duty cycle

4. Experimental results

A DSP controlled PPIBC has been used to experimentally verify the operation of the converter in extended mode. The gate signals in one of the paralleled primary stages have been modified by inserting some control logic circuitry to produce the desired waveforms under extended operation mode. The implemented prototype and the gate drive circuitry are shown in (Figure 8) and (Figure 9) respectively.

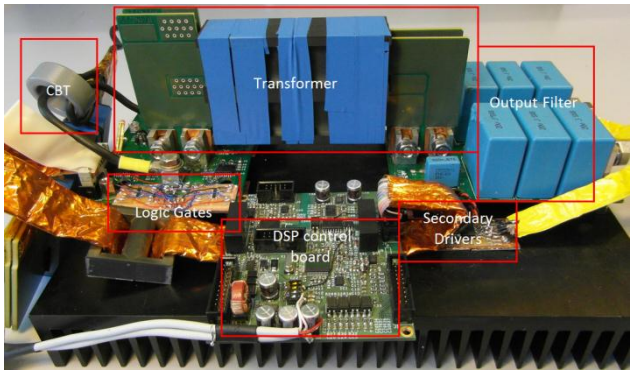
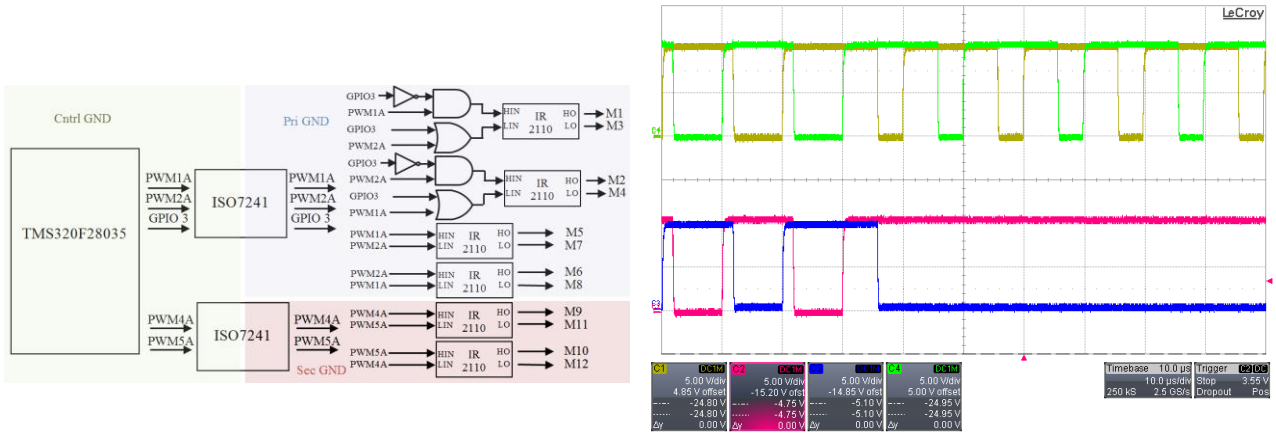


Figure 8. Experimental prototype



(a) (b)

Figure 9. Gate drive circuitry (a) and gate waveforms during normal to extended operating mode transition (b).

(Figure 10) shows a transition event from normal to extended operating mode with pre-calculated duty cycle during converter closed loop operation for an inductor current level equal to 20 A. The change in duty cycle and voltage stress can be observed on one of the primary MOSFETs drain to source voltage waveform. It can be noticed that during extended operation mode the voltage ringing during MOSFET off state increases respect the normal operation mode due to the effect of the leakage inductance of the short circuited transformer.

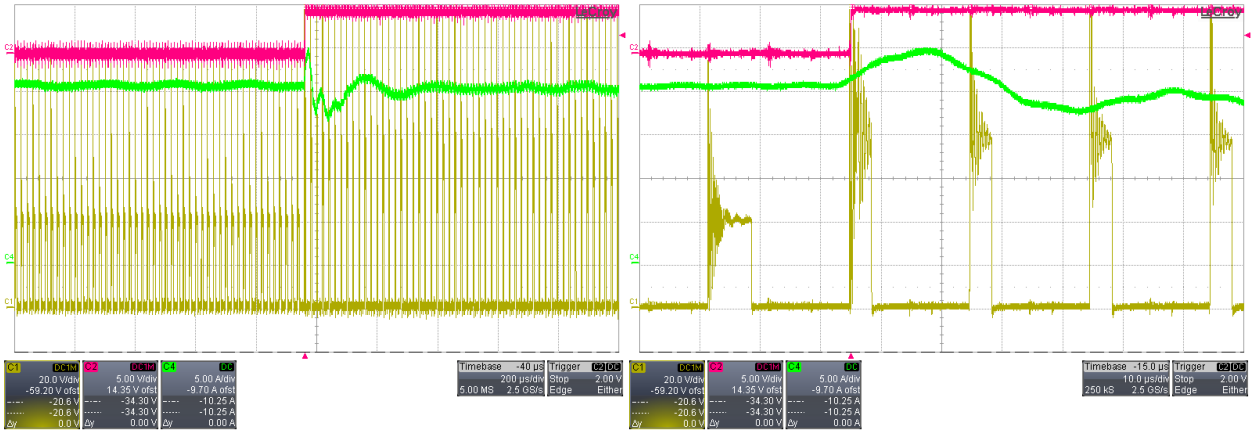


Figure 10. Transition between operating modes with pre-calculated steady state duty cycle (left, time scale:200µs/div) and detailed zoomed of the transition (right, time scale:10µs/div). Source output current I_g (green, 5A/div), primary MOSFET drain to source voltage (brown, 20V/div) and short circuit control signal GPIO3 (red, 5V/div).

5. Conclusions

In applications requiring wide operating voltage ranges, extreme duty cycles and extreme turn ratios for transformers have to be selected for covering the converter specifications which will affect the converter efficiency. Optimizing the converter design for the most probable operating conditions and still covering all the possible operating points is desired. In order to do this a new method for extending the operating voltage range has been proposed for PPIBC where the effective converter voltage conversion ratio is changed by deactivating one of the transformers through short-circuiting its primary windings. This new operation mode has been tested in a series of simulations and experiments where it has been observed that the transition between normal and extended operating modes is a disturbance to the converter due to the change in steady state operating conditions. However, a very smooth transition can be obtained if the steady state duty cycle is pre-calculated based on an accurate model of the converter.

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